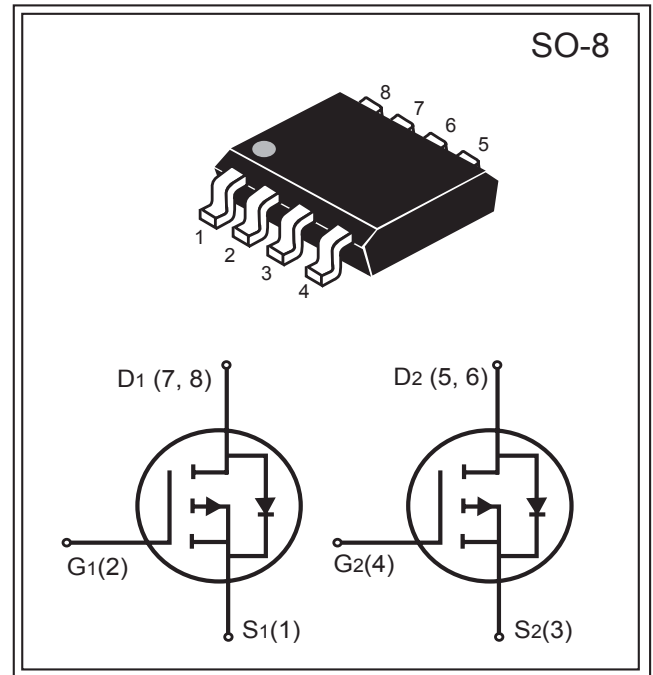




Product Summary		
V <sub>DS</sub> (V)	I <sub>D</sub> (A)	R <sub>DS(ON)</sub> (mΩ) Max
-20V	-5.5A	30 @V <sub>GS</sub> = -4.5V
		45 @V <sub>GS</sub> = -2.5V
		90 @V <sub>GS</sub> = -1.8V

### FEATURES

- ◆ Super high density cell design for low R<sub>DS(ON)</sub>.
- ◆ Rugged and reliable.
- ◆ SO-8 package.
- ◆ Pb free.



### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	-20	V
Gate-Source Voltage	V <sub>GS</sub>	±10	V
Drain Current-Continuous @ T <sub>J</sub> = 125°C	I <sub>D</sub>	-5.5	A
-Pulsed <sup>b</sup>	I <sub>DM</sub>	-15	A
Drain-Source Diode Forward Current <sup>a</sup>	I <sub>S</sub>	-1.7	A
Maximum Power Dissipation <sup>a</sup>	P <sub>D</sub>	2.0	W
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to 150	°C

### THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient <sup>a</sup>	R <sub>θJA</sub>	62.5	°C/W
--	------------------	------	------

South Sea Semiconductor reserves the right to make changes to improve reliability or manufacturability without advance notice.

South Sea Semiconductor, January 2008 (Rev 1.0)



P-Channel Electrical Characteristics (TA = 25°C unless otherwise noted)						
Parameter	Symbol	Condition	Min	Typ <sup>c</sup>	Max	Unit
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =-250 μA	-20			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-16V, V <sub>GS</sub> =0V			-1	μA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> =±8V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> I <sub>D</sub> =-250 μA	-0.4		-1.0	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-6.0A		23	30	mΩ
		V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-3.0A		38	45	
		V <sub>GS</sub> =-1.8V, I <sub>D</sub> =-2.0A			90	
On-State Drain Current	I <sub>D(ON)</sub>	V <sub>DS</sub> =-5V, V <sub>GS</sub> =-4.5V	-10			A
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =-5V, I <sub>D</sub> =-4A		10		S
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =-6V		1100		pF
Output Capacitance	C <sub>OSS</sub>	V <sub>GS</sub> =0V		240		
Reverse Transfer Capacitance	C <sub>RSS</sub>	f=1.0MHz		170		
Turn-On Delay Time	t <sub>D(ON)</sub>	V <sub>DD</sub> =-6V,		25		ns
Rise Time	t <sub>r</sub>	I <sub>D</sub> =-1A,		45		
Turn-Off Delay Time	t <sub>D(OFF)</sub>	V <sub>GEN</sub> =-4.5V,		80		
Fall Time	t <sub>f</sub>	R <sub>GEN</sub> =6Ω,		60		
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =-6V,		13		nC
Gate-Source Charge	Q <sub>gs</sub>	I <sub>D</sub> =-3.4A,		2		
Gate-Drain Charge	Q <sub>gd</sub>	V <sub>GS</sub> =-4.5V		3.8		
Diode Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =-1.7A			-1.2	V

Notes :

- a. Surface Mounted on FR4 Board, t ≤ 10 sec.
- b. Pulse Test : Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
- c. Guaranteed by design, not subject to production testing.

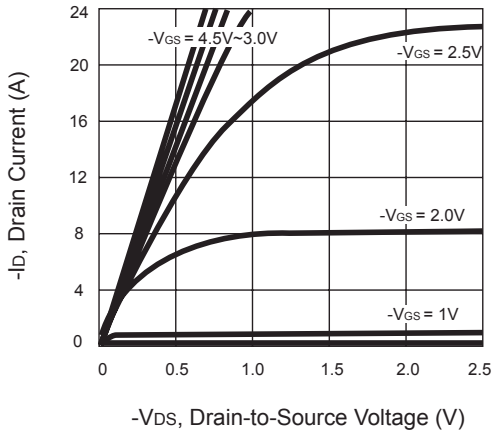


Figure 1. Output Characteristics

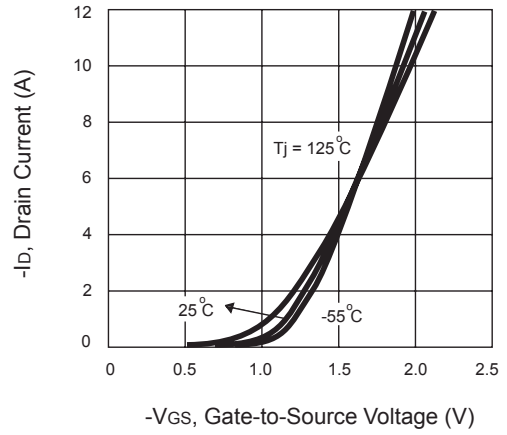


Figure 2. Transfer Characteristics

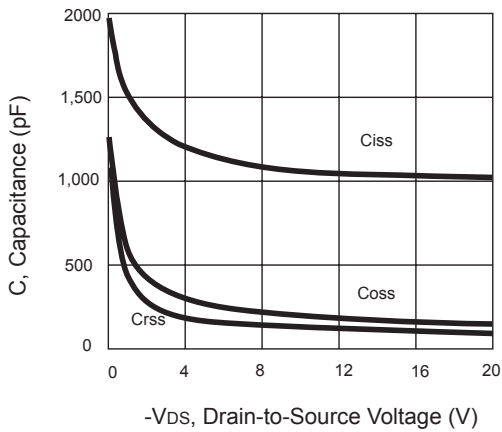


Figure 3. Capacitance

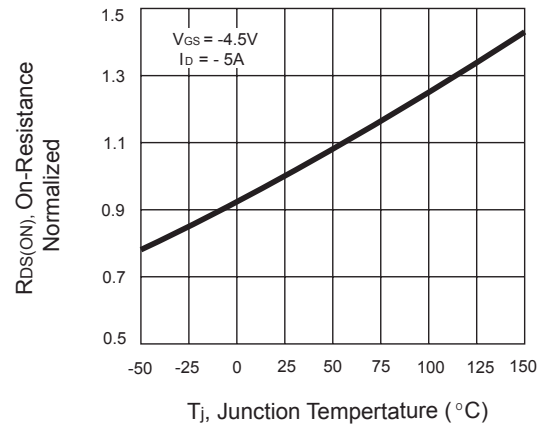


Figure 4. On-Resistance Variation with Temperature

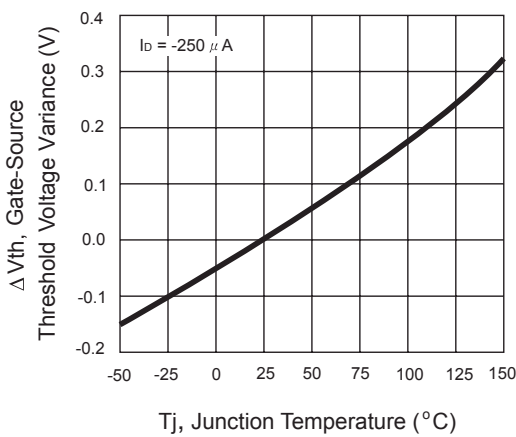


Figure 5. Gate Threshold Variation with Temperature

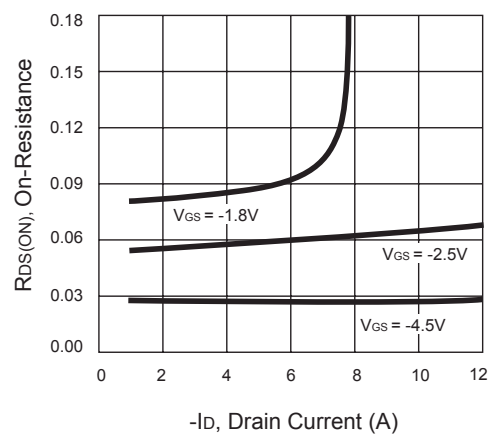
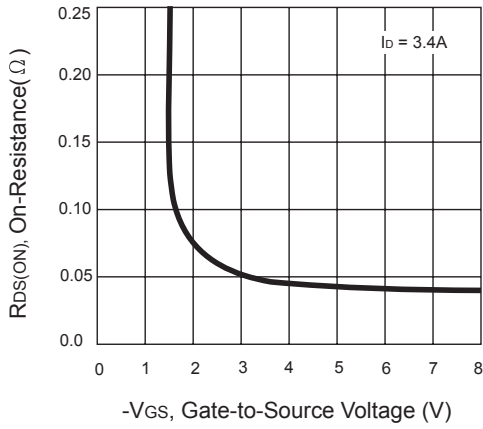
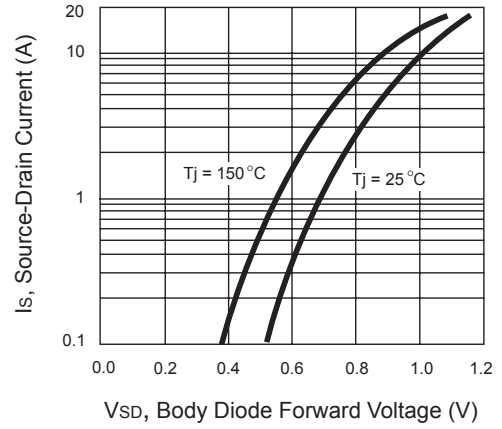


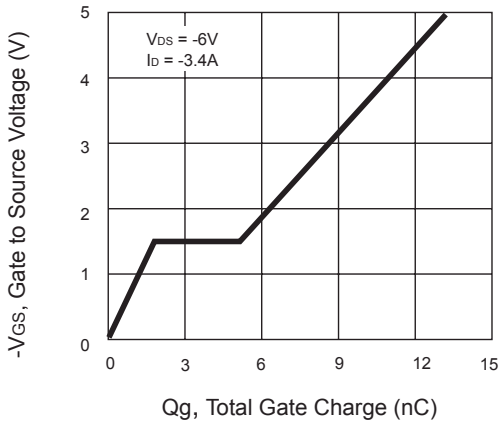
Figure 6. On-Resistance Variation with Drain Current



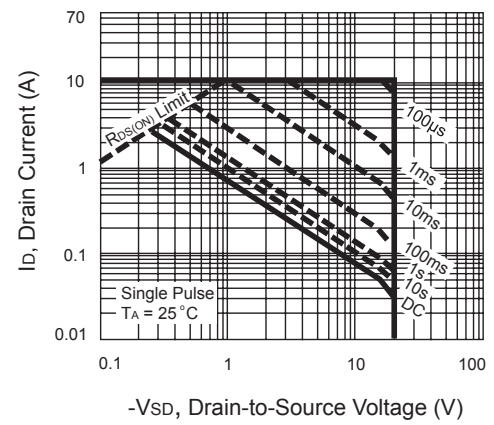
**Figure 7. On-Resistance Variation with Gate-to-Source Voltage**



**Figure 8. Body Diode Forward Voltage Variation with Source Current**



**Figure 9. Gate Charge**



**Figure 10. Maximum Safe Operating Area**

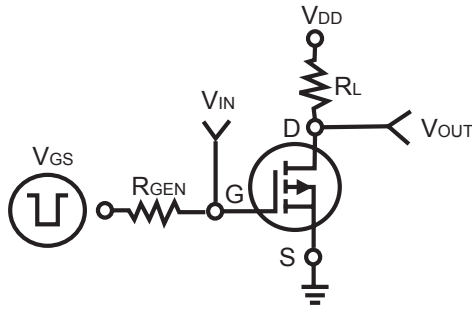


Figure 11. Switching Test Circuit

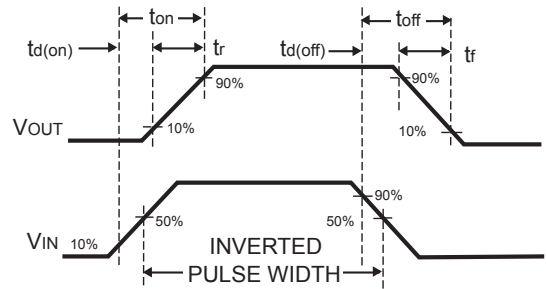


Figure 12. Switching Waveforms

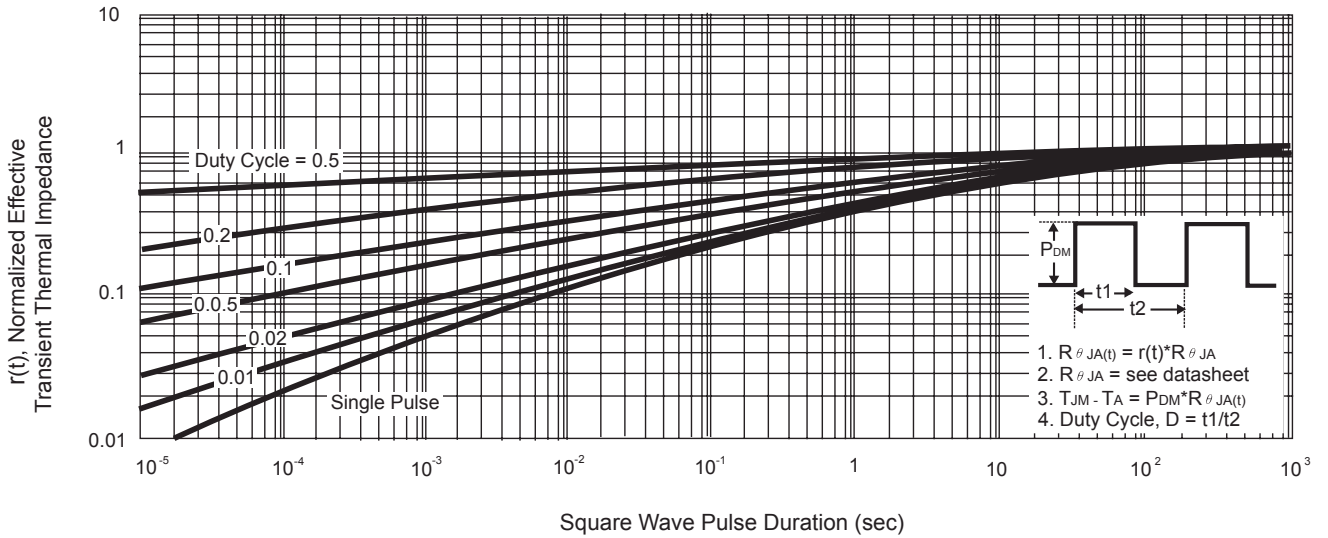


Figure 13. Normalized Thermal Transient Impedance Curve