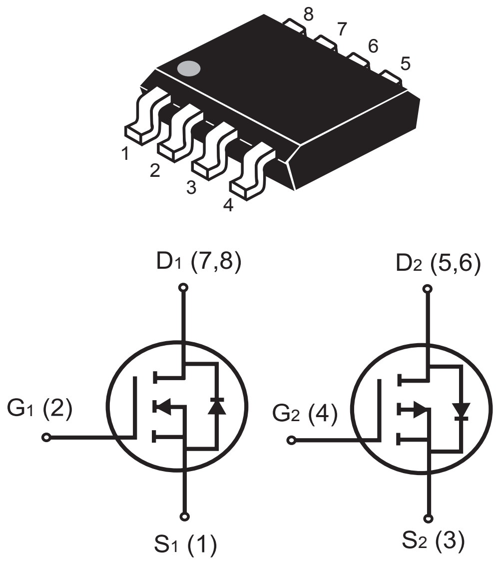
SSM8958

Dual Enhancement Mode MOSFET

Product Summary (N-Channel)		
V_{DS} (V)	I_D (A)	$R_{DS(ON)}$ (mΩ) Max
30V	6A	30 @V_{GS} = 10V
		60 @V_{GS} = 4.5V

Product Summary (P-Channel)		
V_{DS} (V)	I_D (A)	$R_{DS(ON)}$ (mΩ) Max
- 30V	- 4.5A	60 @V_{GS} = - 10V
		100 @V_{GS} = - 4.5V

SO-8



ABSOLUTE MAXIMUM RATINGS (T_A = 25℃ unless otherwise noted)

Parameter	Symbol	N-Channel Limited	P-Channel Limited	Unit
Drain-Source Voltage	V_{DS}	30	-30	V
Gate-Source Voltage	V_{GS}	±25	±20	V
Drain Current-Continuous @ T_J = 25°C	I_D	6	-4.5	A
-Pulsed [b]	I_{DM}	25	-23	A
Drain-Source Diode Forward Current [a]	I_S	1.7	-1.7	A
Maximum Power Dissipation [a]	P_D	2.0		W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150		°C

THERMAL CHRACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient [a]	$R_{\theta JA}$	62.5	°C/W

N-Channel Electrical Characteristics (T_A = 25℃ unless otherwise noted)						
Parameter	Symbol	Condition	Min	Typ[c]	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250 μA	30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=24V, V_{GS}=0V			1	μA
Gate-Body Leakage	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS} I_D=250 μA	1	1.7	2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=6A			30	mΩ
		V_{GS}=4.5V, I_D=5A			60	
On-State Drain Current	$I_{D(ON)}$	V_{DS}=5V, V_{GS}=10V	15			A
Forward Transconductance	g_{FS}	V_{DS}=5V, I_D=6A		9		S
Input Capacitance	C_{ISS}	V_{DS}=15V V_{GS}=0V f=1.0MHz		750		pF
Output Capacitance	C_{OSS}			120		
Reverse Transfer Capacitance	C_{RSS}			80		
Turn-On Delay Time	$t_{D(ON)}$	V_{DD}=15V, I_D=1A, V_{GS}=10V, R_{GEN}=10Ω,		16		ns
Rise Time	t_r			7		
Turn-Off Delay Time	$t_{D(OFF)}$			22		
Fall Time	t_f			10		
Total Gate Charge	Q_g	V_{DS}=15V, I_D=1A, V_{GS}=10V		12		nC
		V_{DS}=15V, I_D=1A, V_{GS}=4.5V		6.5		
Gate-Source Charge	Q_{gs}	V_{DS}=15V, I_D=1A, V_{GS}=10V		2.5		
Gate-Drain Charge	Q_{gd}			2		
Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_D=1.7A		0.7	1.2	V

Notes：
a. Surface Mounted on FR4 Board, t ≤10 sec.
b. Pulse Test：Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
c. Guaranteed by design, not subject to production testing.

P-Channel Electrical Characteristics (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ[c]	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=-250 μA	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-24V, V_{GS}=0V			-1	μA
Gate-Body Leakage	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS} I_D=-250 μA	-1	-1.5	-2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-4.9A			60	mΩ
		V_{GS}=-4.5V, I_D=-3.6A			100	
On-State Drain Current	$I_{D(ON)}$	V_{DS}=-5V, V_{GS}=-10V	-20			A
Forward Transconductance	g_{FS}	V_{DS}=-5V, I_D=-4.9A	3.5			S
Input Capacitance	C_{ISS}	V_{DS}=-15V V_{GS}=0V f=1.0MHz		560		pF
Output Capacitance	C_{OSS}			130		
Reverse Transfer Capacitance	C_{RSS}			90		
Turn-On Delay Time	$t_{D(ON)}$	V_{DD}=-15V, I_D=-1A, V_{GEN}=-10V, R_{GEN}=6Ω, R_L=15Ω		11		ns
Rise Time	t_r			12.2		
Turn-Off Delay Time	$t_{D(OFF)}$			56		
Fall Time	t_f			33.3		
Total Gate Charge	Q_g	V_{DS}=-15V, I_D=-4.9A, V_{GS}=-10V		13		nC
		V_{DS}=-15V, I_D=-4.9A, V_{GS}=-4.5V		8		
Gate-Source Charge	Q_{gs}	V_{DS}=-15V, I_D=-4.9A, V_{GS}=-10V		2.5		
Gate-Drain Charge	Q_{gd}			2.5		
Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_D=-1.7A		-0.8	-1.2	V

Notes：
- a. Surface Mounted on FR4 Board, t ≤10 sec.
- b. Pulse Test：Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
- c. Guaranteed by design, not subject to production testing.

N-Channel

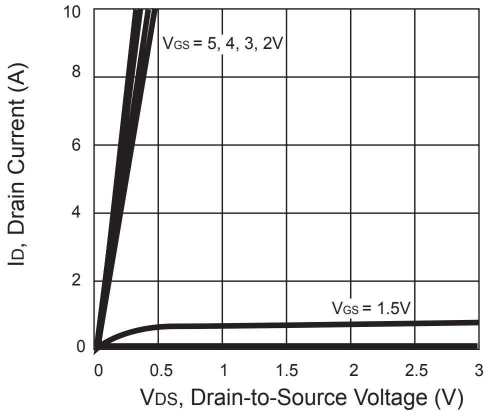


Figure 1. Output Characteristics

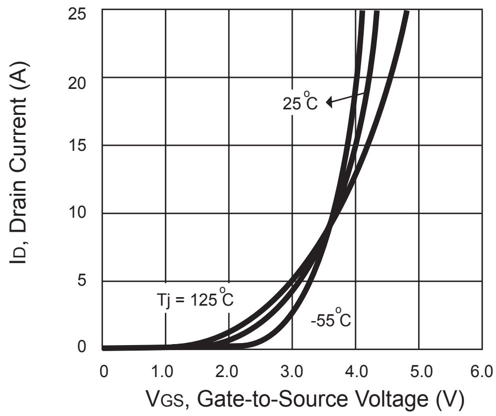


Figure 2. Transfer Characteristics

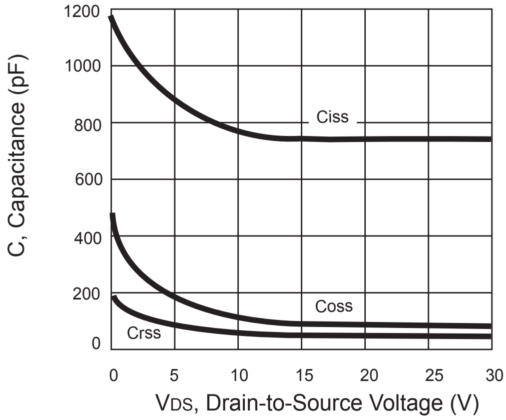
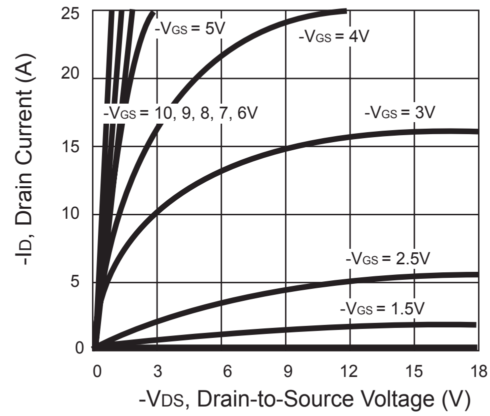


Figure 3. Capacitance

P-Channel



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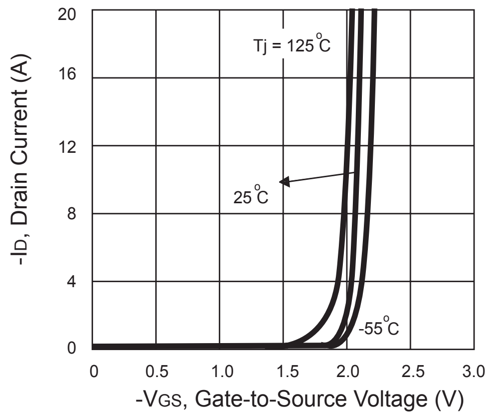

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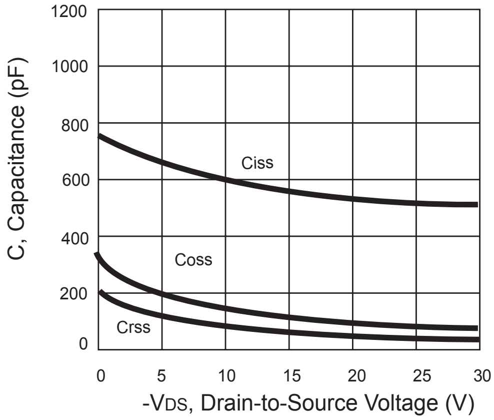

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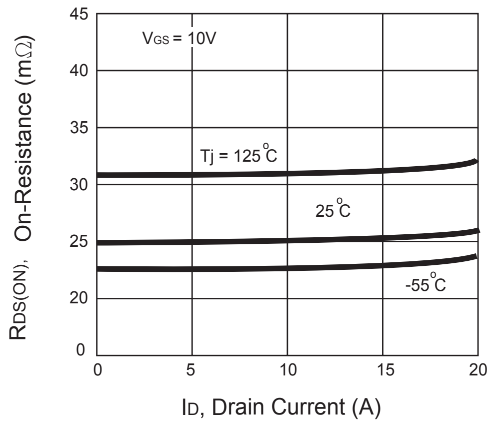
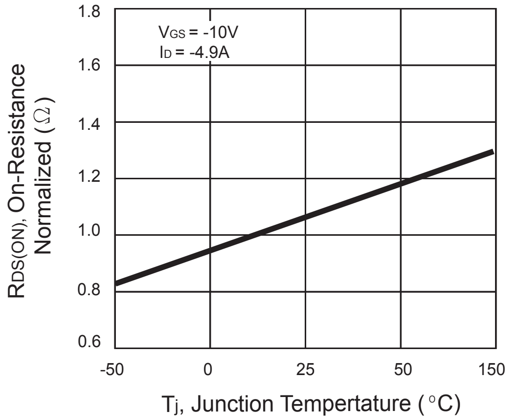


Figure 4. On-Resistance Variation with Temperature



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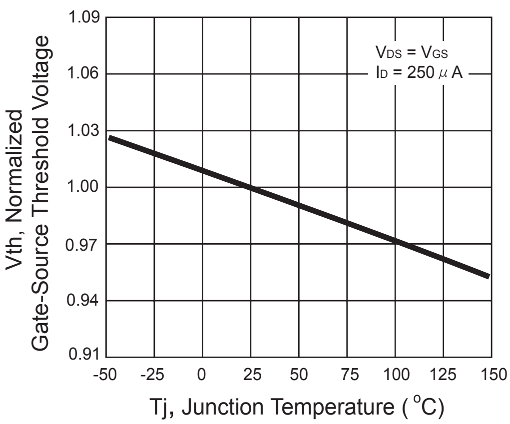
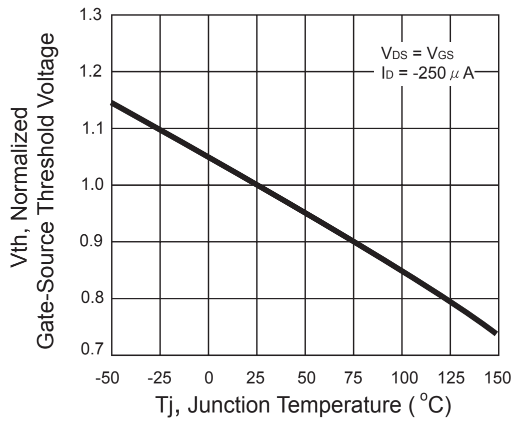


Figure 5. Gate Threshold Variation with Temperature



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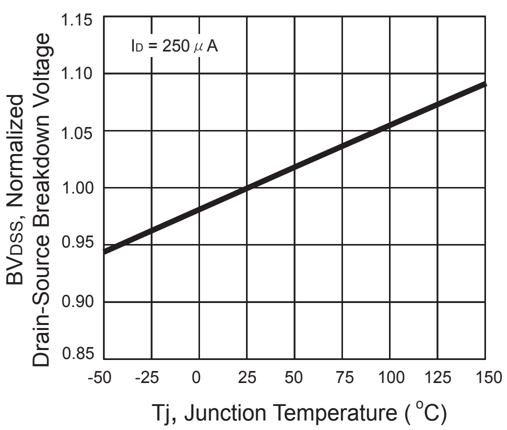
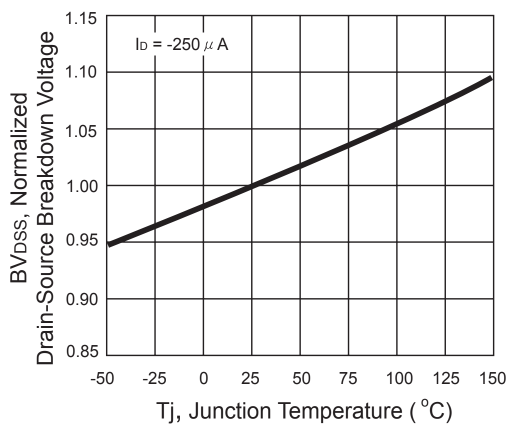


Figure 6. Breakdown Voltage Variation with Temperature



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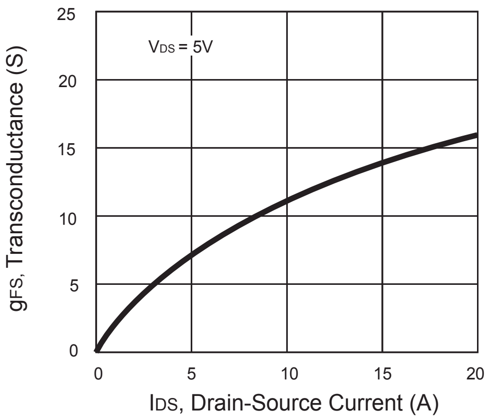


Figure 7. Transconductance Variation with Drain Current

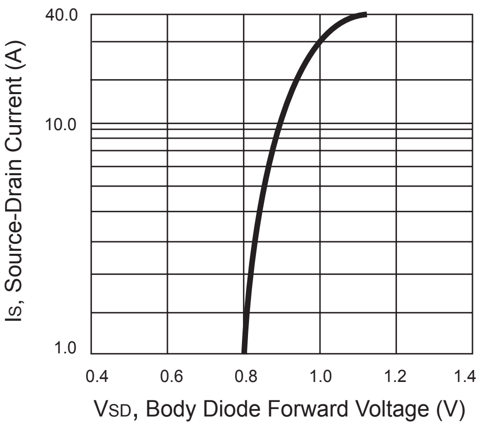


Figure 8. Body Diode Forward Voltage Variation with Source Current

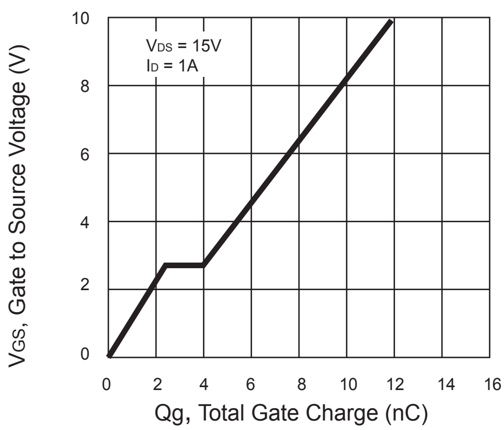
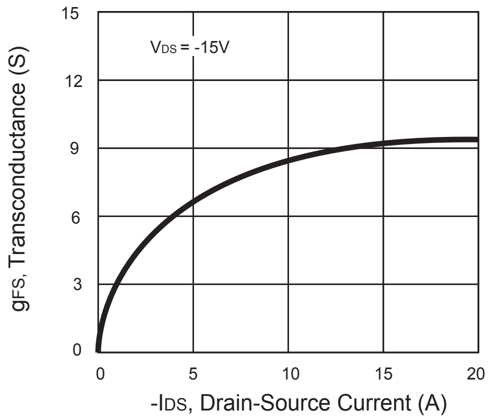


Figure 9. Gate Charge

P-Channel



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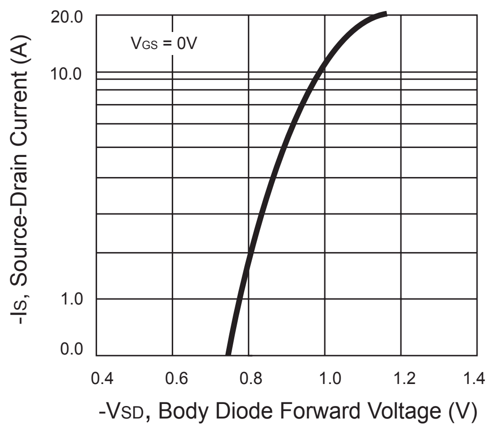

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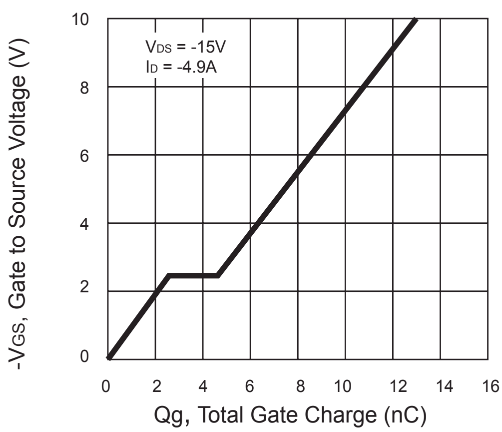

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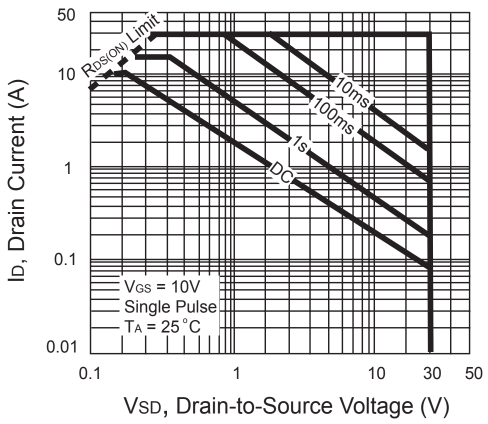
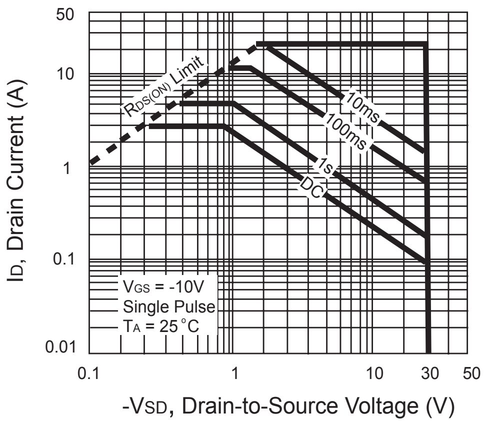


Figure 10. Maximum Safe Operating Area

P-Channel



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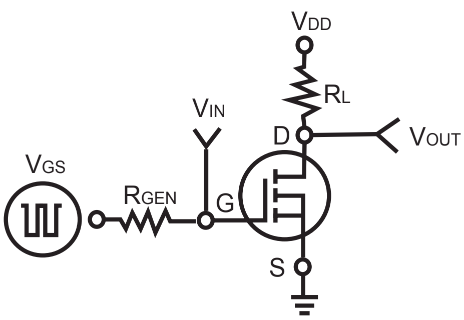


Figure 11. Switching Test Circuit

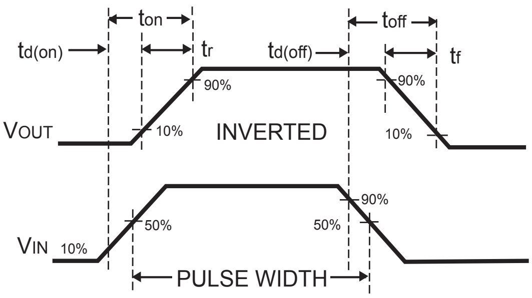


Figure 12. Switching Waveforms

N-Channel

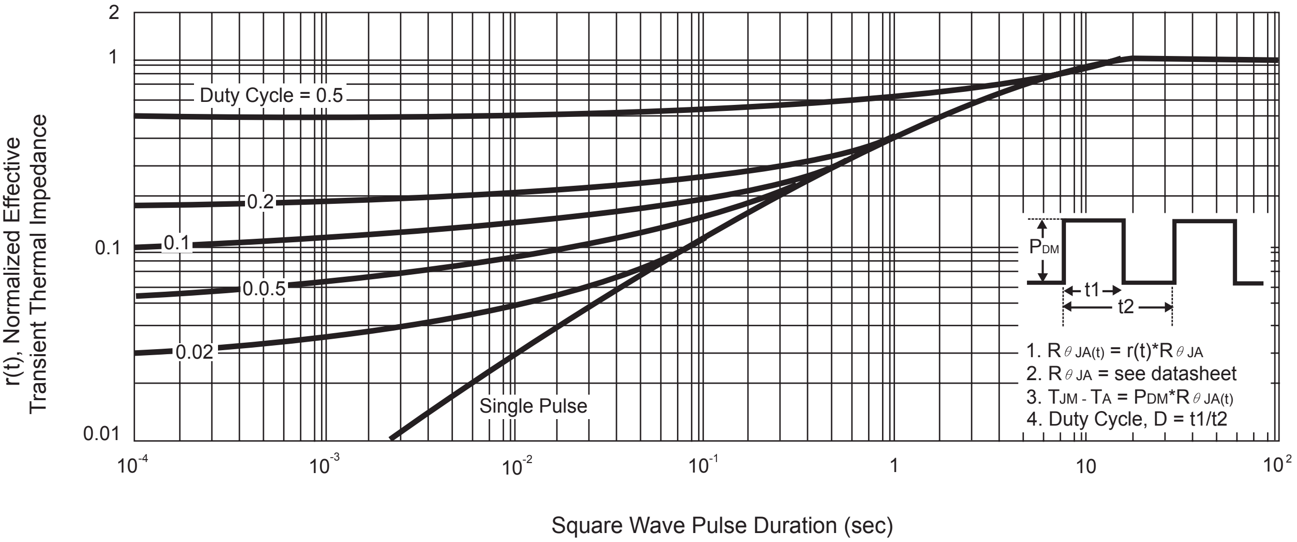
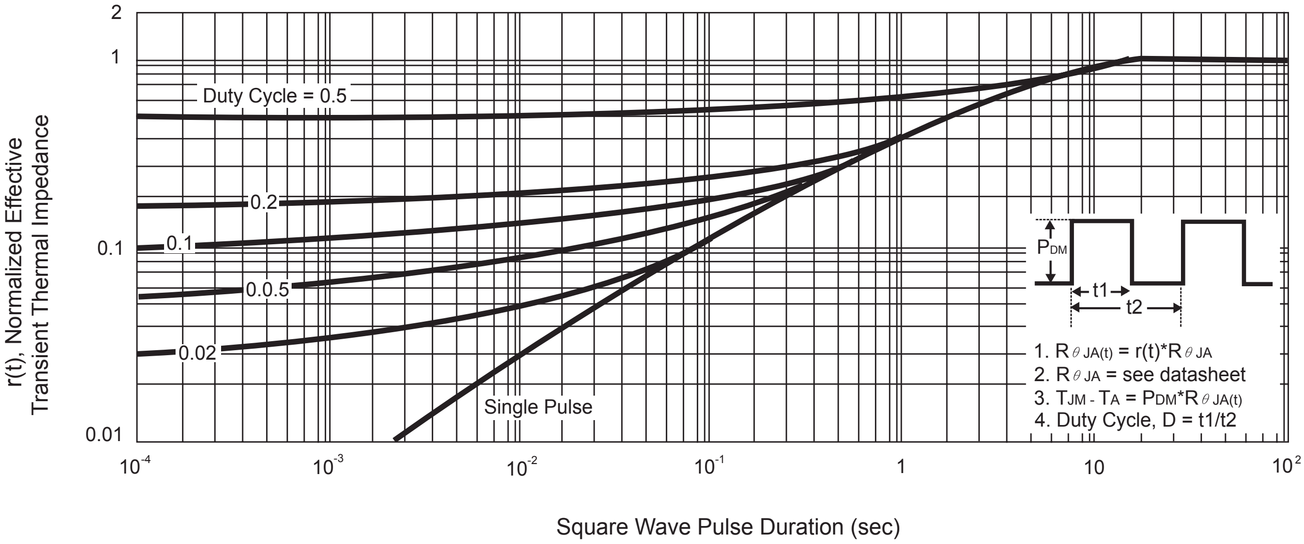


Figure 13. Normalized Thermal Transient Impedance Curve

P-Channel



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