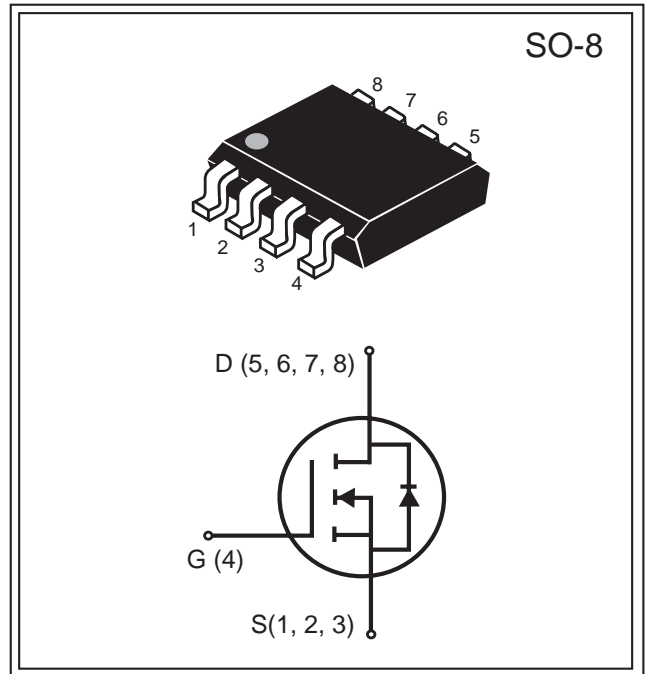




Product Summary		
V <sub>DS</sub> (V)	I <sub>D</sub> (A)	R <sub>DS(ON)</sub> (mΩ) Max
30V	6.3A	25 @V <sub>GS</sub> = 10V
		45 @V <sub>GS</sub> = 4.5V

### FEATURES

- Super high dense cell design for low R<sub>DS(ON)</sub>.
- Rugged and reliable.
- Surface Mount package.



ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C unless otherwise noted)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	30	V
Gate-Source Voltage	V <sub>GS</sub>	±20	V
Drain Current-Continuous @ T <sub>J</sub> = 25 °C	I <sub>D</sub>	6.3	A
-Pulsed <sup>b</sup>	I <sub>DM</sub>	25	A
Drain-Source Diode Forward Current <sup>a</sup>	I <sub>S</sub>	1.7	A
Maximum Power Dissipation <sup>a</sup>	P <sub>D</sub>	2.5	W
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to 150	°C
THERMAL CHARACTERISTICS			
Thermal Resistance, Junction-to-Ambient <sup>a</sup>	R <sub>JA</sub>	50	°C/W

South Sea Semiconductor reserves the right to make changes to improve reliability or manufacturability without advance notice.



P-Channel Electrical Characteristics (TA = 25°C unless otherwise noted)						
Parameter	Symbol	Condition	Min	Typ <sup>c</sup>	Max	Unit
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250 μ A	30			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =24V, V <sub>GS</sub> =0V			1	μ A
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20V, V <sub>DS</sub> =0V			± 100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> I <sub>D</sub> =250 μ A	1	1.7	2.5	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =6A			25	m
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =5A			45	
On-State Drain Current	I <sub>D(ON)</sub>	V <sub>DS</sub> =5V, V <sub>GS</sub> =10V	15			A
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =6A		9		S
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =15V V <sub>GS</sub> =0V f=1.0MHz		828		PF
Output Capacitance	C <sub>OSS</sub>			141		
Reverse Transfer Capacitance	C <sub>RSS</sub>			100		
Turn-On Delay Time	t <sub>D(ON)</sub>	V <sub>DD</sub> =15V, I <sub>D</sub> =1A, V <sub>GS</sub> =10V, R <sub>GEN</sub> =10 Ω		16		ns
Rise Time	t <sub>r</sub>			7		
Turn-Off Delay Time	t <sub>D(OFF)</sub>			22		
Fall Time	t <sub>f</sub>			10		
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =15V, I <sub>D</sub> =1A, V <sub>GS</sub> =10V		16		nC
		V <sub>DS</sub> =15V, I <sub>D</sub> =1A, V <sub>GS</sub> =4.5V		7.5		
Gate-Source Charge	Q <sub>gs</sub>	V <sub>DS</sub> =15V, I <sub>D</sub> =1A, V <sub>GS</sub> =10V		3		
Gate-Drain Charge	Q <sub>gd</sub>			3		
Diode Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =1.7A		0.8	1.2	V

Notes :

- a. Surface Mounted on FR4 Board, t ≤ 10 sec.
- b. Pulse Test : Pulse Width ≤ 300 μ s, Duty Cycle ≤ 2%.
- c. Guaranteed by design, not subject to production testing.

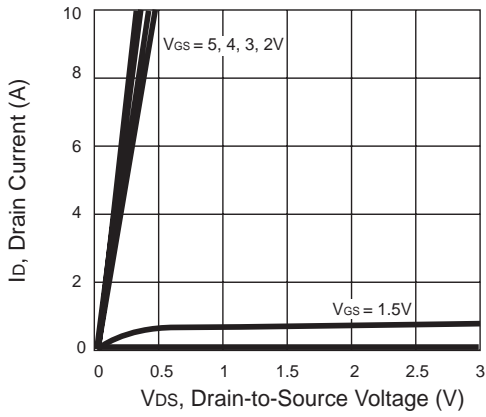


Figure 1. Output Characteristics

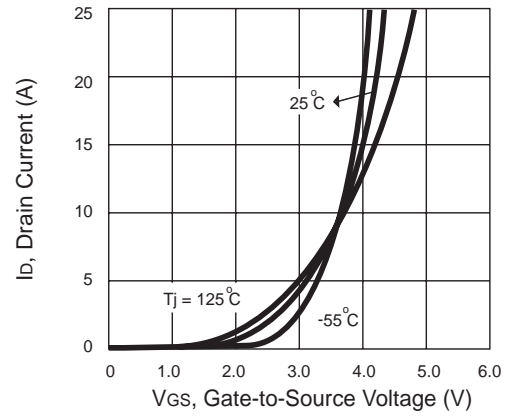


Figure 2. Transfer Characteristics

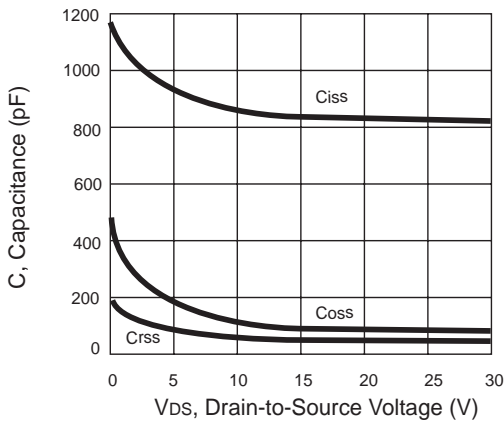


Figure 3. Capacitance

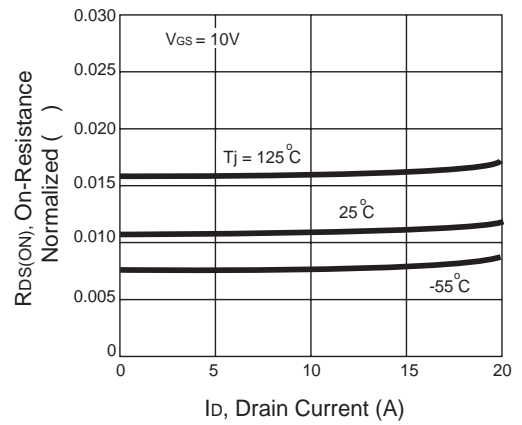


Figure 4. On-Resistance Variation with Temperature

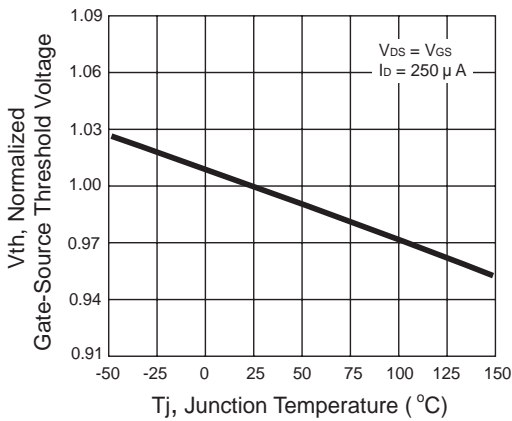


Figure 5. Gate Threshold Variation with Temperature

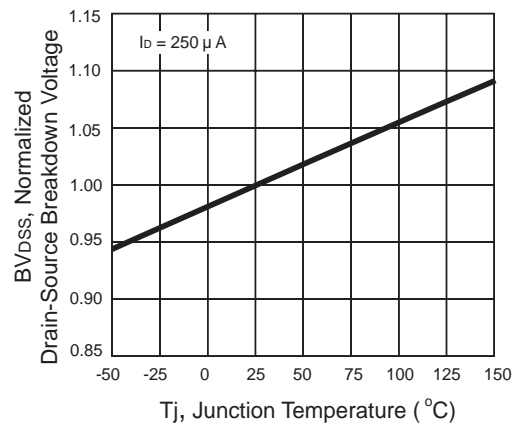
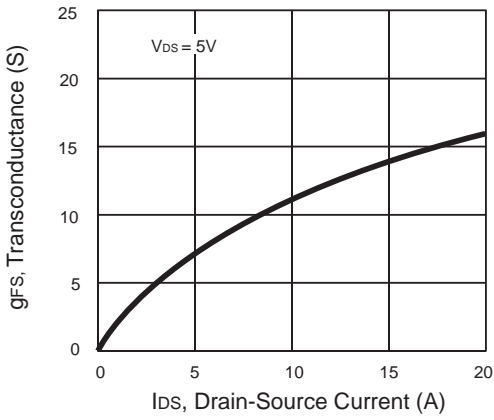
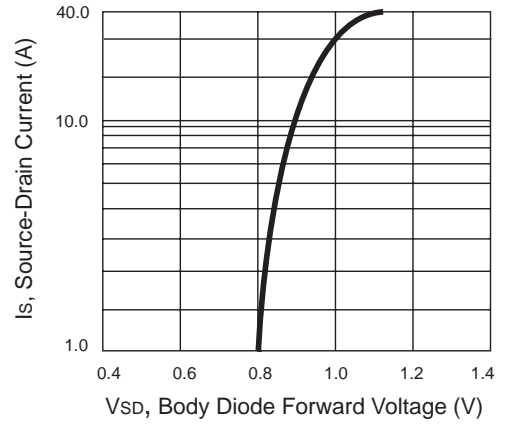


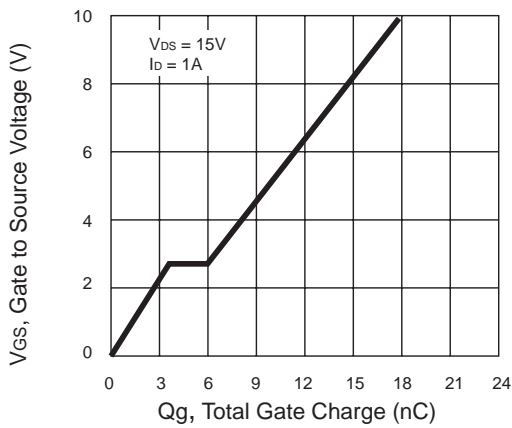
Figure 6. Breakdown Voltage Variation with Temperature



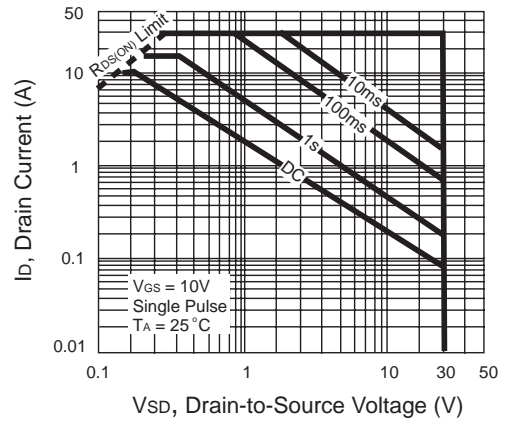
**Figure 7. Transconductance Variation with Drain Current**



**Figure 8. Body Diode Forward Voltage Variation with Source Current**



**Figure 9. Gate Charge**



**Figure 10. Maximum Safe Operating Area**

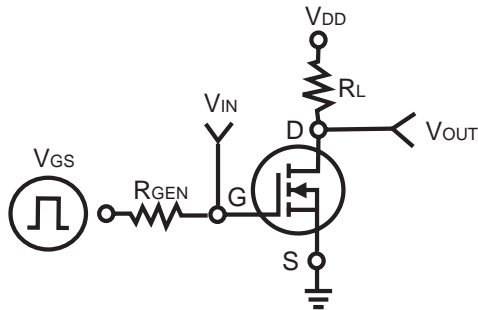


Figure 11. Switching Test Circuit

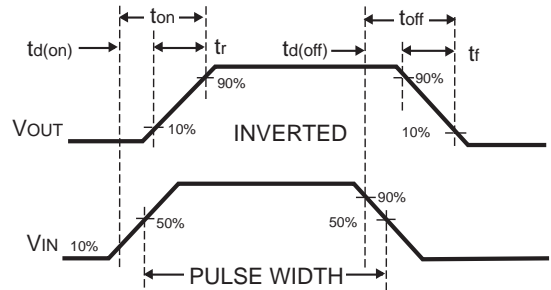


Figure 12. Switching Waveforms

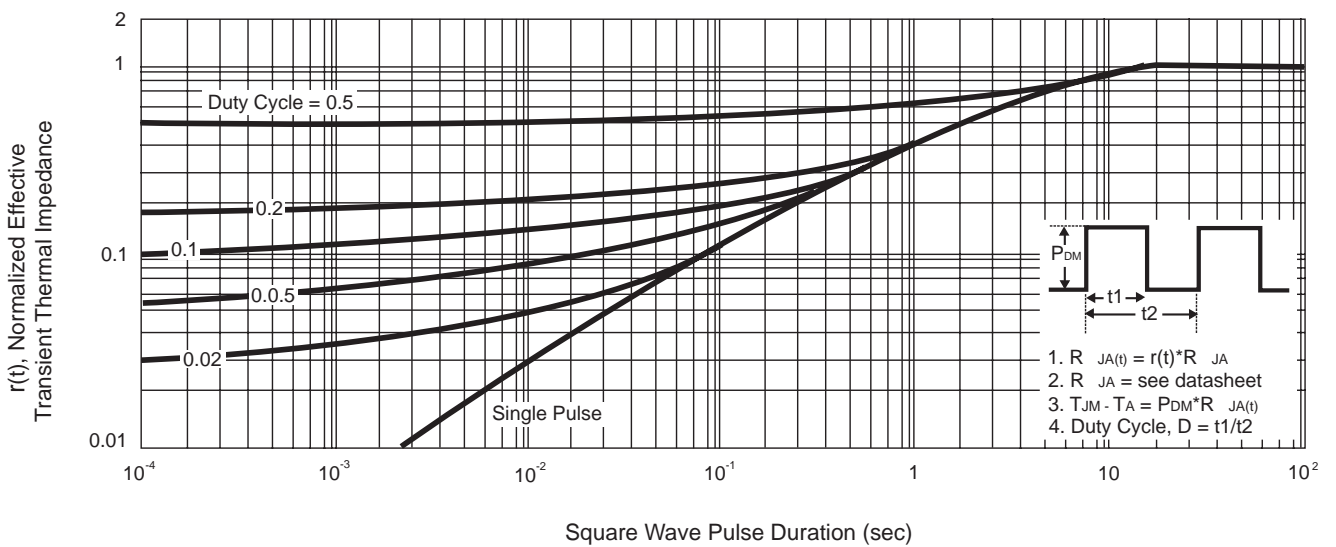


Figure 13. Normalized Thermal Transient Impedance Curve