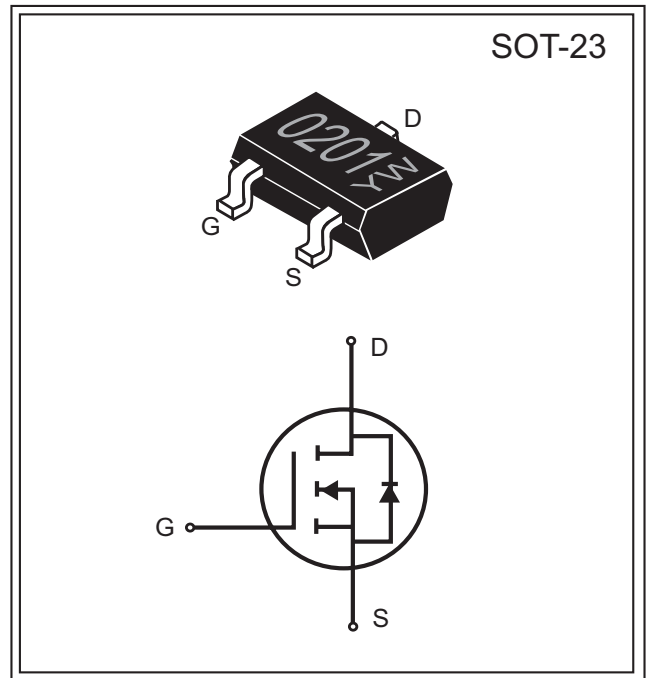




Product Summary		
V <sub>DS</sub> (V)	I <sub>D</sub> (A)	R <sub>DS(ON)</sub> (Ω) Max
20V	0.5A	1.3 @V <sub>GS</sub> = 10V
		1.6 @V <sub>GS</sub> = 4.5V



### FEATURES

- ◆ Super high dense cell design for low R<sub>DS(ON)</sub>.
- ◆ Rugged and reliable.
- ◆ SOT-23 package.
- ◆ Pb Free.

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25°C unless otherwise noted)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	20	V
Gate-Source Voltage	V <sub>GS</sub>	±20	V
Drain Current-Continuous @ T <sub>c</sub> = 25°C	I <sub>D</sub>	0.5	A
-Pulsed <sup>b</sup>	I <sub>DM</sub>	0.8	A
Drain-Source Diode Forward Current <sup>a</sup>	I <sub>S</sub>	0.5	A
Maximum Power Dissipation <sup>a</sup>	P <sub>D</sub>	0.35	W
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to 150	°C
THERMAL CHARACTERISTICS			
Thermal Resistance, Junction-to-Ambient <sup>a</sup>	R <sub>θJA</sub>	357	°C/W

South Sea Semiconductor reserves the right to make changes to improve reliability or manufacturability without advance notice.



Electrical Characteristics (T <sub>A</sub> = 25°C unless otherwise noted)						
Parameter	Symbol	Condition	Min	Typ <sup>c</sup>	Max	Unit
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250 μA	20			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V			1	μA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> I <sub>D</sub> =250 μA	1.0	1.5	3.0	V
Drain-Source On-State Resistance	R <sub>Ds(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =0.3A			1.3	Ω
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =0.1A			1.6	
On-State Drain Current	I <sub>D(ON)</sub>	V <sub>DS</sub> =10V, V <sub>GS</sub> =10V	0.5			A
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =0.3A		550		mS
Input Capacitance	C <sub>iSS</sub>	V <sub>DS</sub> =12V V <sub>GS</sub> =0V f=1.0MHz		33		pF
Output Capacitance	C <sub>oSS</sub>			19		
Reverse Transfer Capacitance	C <sub>rSS</sub>			6.5		
Turn-On Delay Time	t <sub>D(ON)</sub>	V <sub>DD</sub> =15V, I <sub>D</sub> =0.3A, V <sub>GEN</sub> =10V, R <sub>GEN</sub> =6 Ω, R <sub>L</sub> =50 Ω		4	8	ns
Rise Time	t <sub>r</sub>			8	15	
Turn-Off Delay Time	t <sub>D(OFF)</sub>			9	15	
Fall Time	t <sub>f</sub>			6	12	
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =16V, I <sub>D</sub> =0.3A, V <sub>GS</sub> =10V		900	1500	pC
Gate-Source Charge	Q <sub>gs</sub>			200		
Gate-Drain Charge	Q <sub>gd</sub>			200		
Diode Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =0.3A		0.85	1.2	V

Notes :

- a. Surface Mounted on FR4 Board, t ≤ 10 sec.
- b. Pulse Test : Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
- c. Guaranteed by design, not subject to production testing.

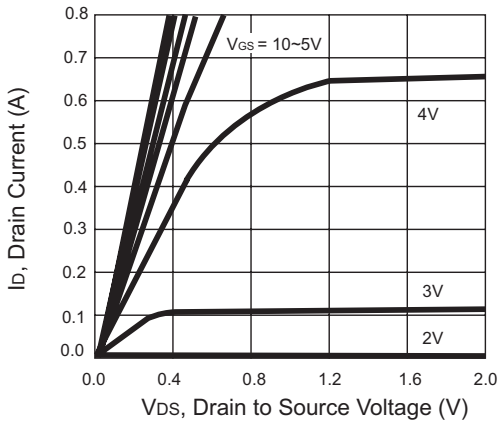


Figure 1. Output Characteristics

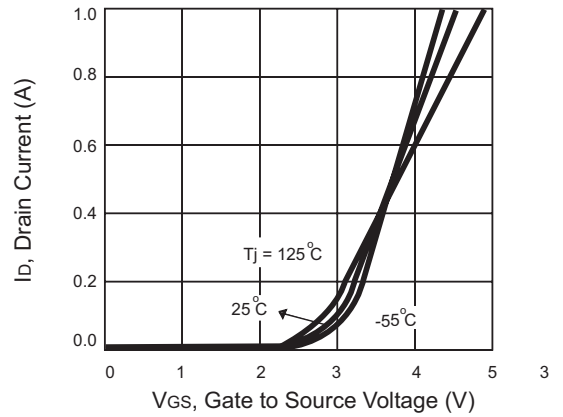


Figure 2. Transfer Characteristics

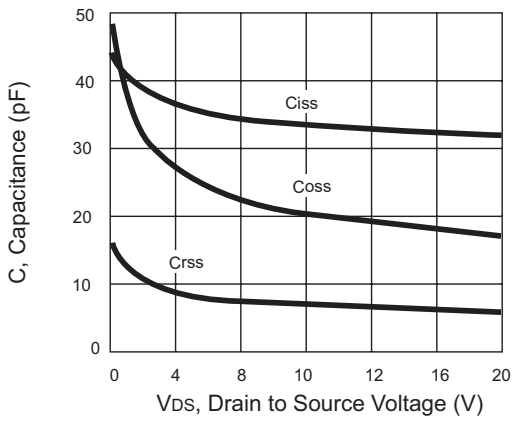


Figure 3. Capacitance

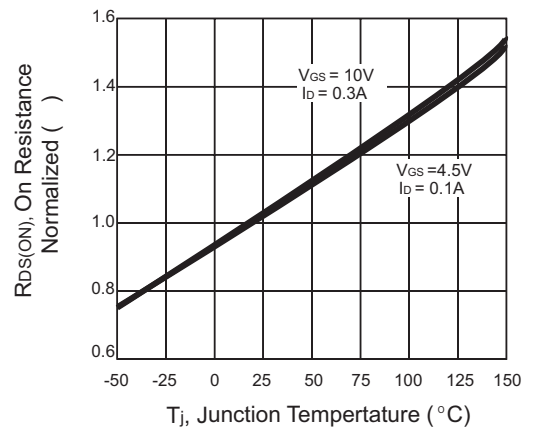


Figure 4. On Resistance Variation with Junction Temperature

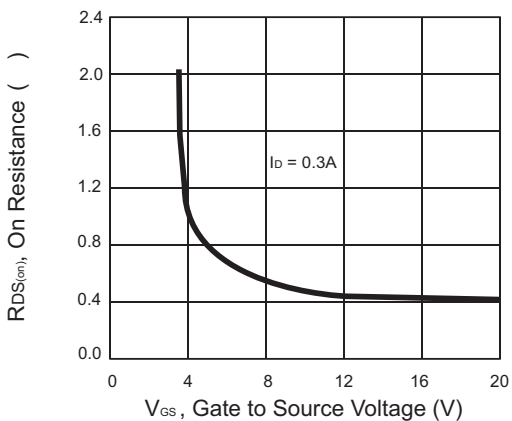


Figure 5. On Resistance Variation with Gate to Source Voltage

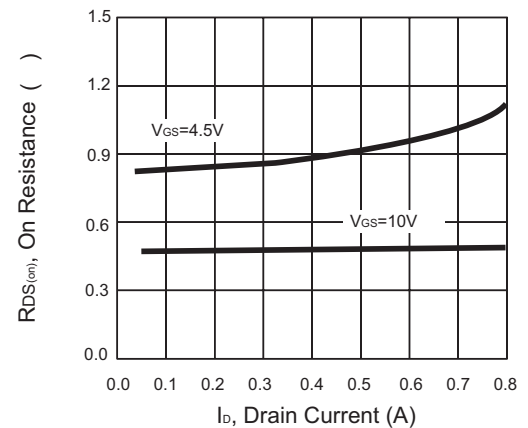


Figure 6. On Resistance Variation with Drain Current

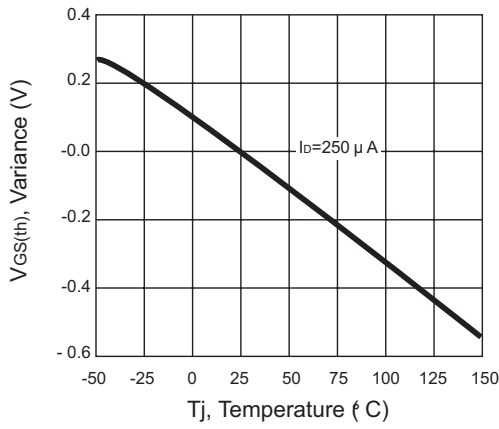


Figure 7. Threshold Voltage

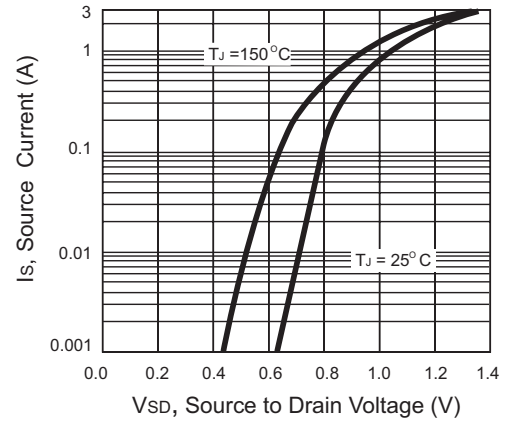


Figure 8. Source Drain Diode Forward Voltage

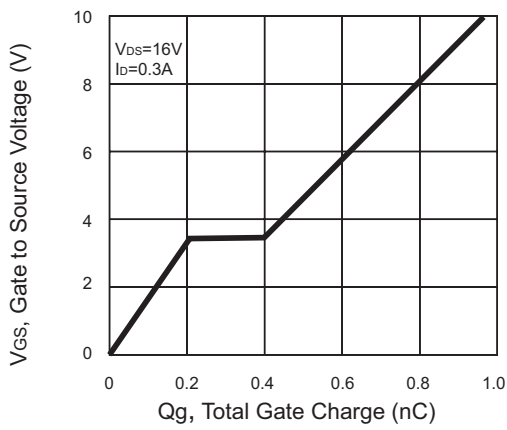


Figure 9. Gate Charge

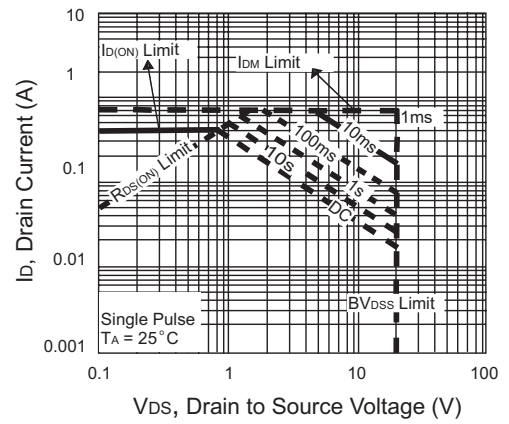


Figure 10. Safe Operating Area

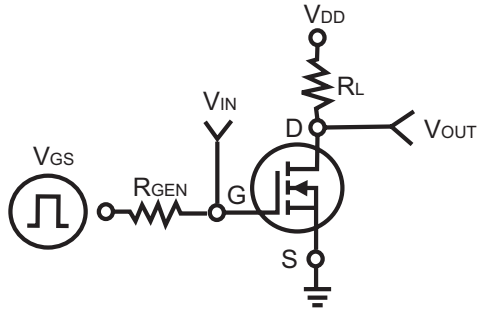


Figure 11. Switching Test Circuit

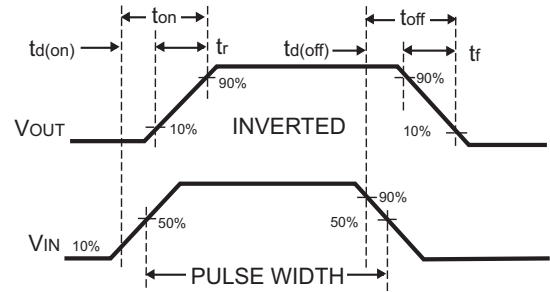


Figure 12. Switching Waveforms

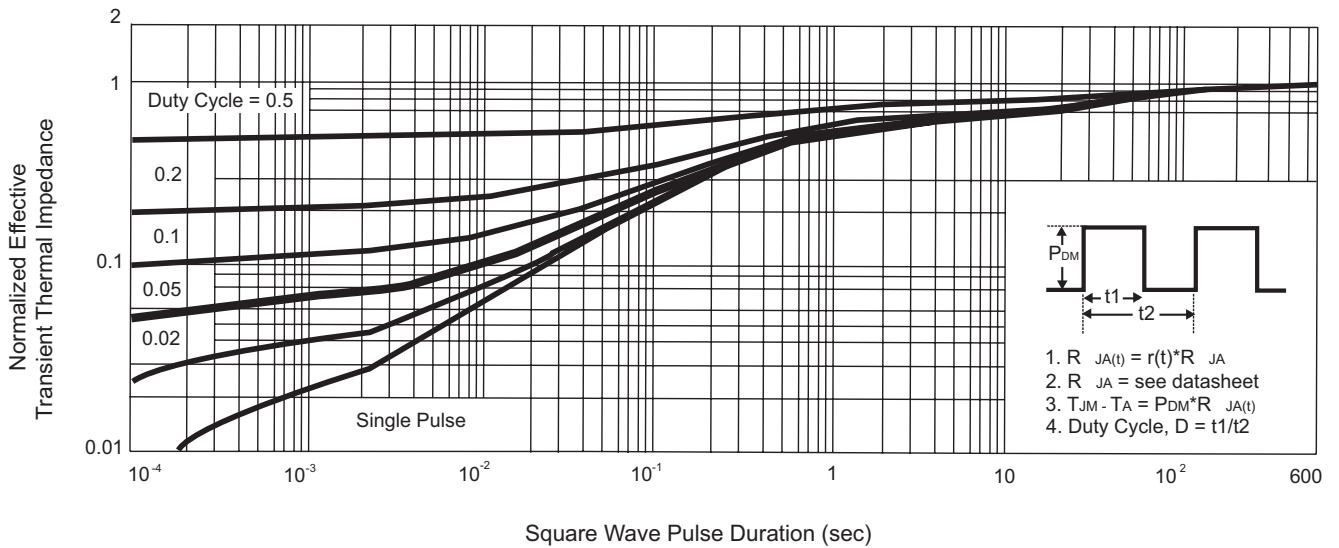


Figure 13. Normalized Thermal Transient Impedance Curve, Junction to Ambient