



South Sea Semiconductor

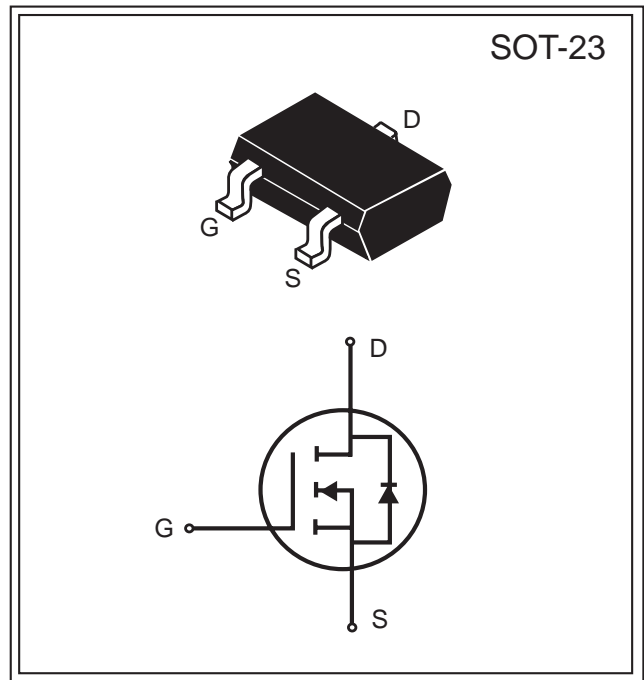
SSS2312A

N-Channel Enhancement Mode MOSFET

| Product Summary | | |
|---------------------|--------------------|------------------------------|
| V _{DS} (V) | I _D (A) | R _{DS(ON)} (mΩ) Max |
| 20V | 3.77A | 33 @V _{GS} = 4.5V |
| | | 40 @V _{GS} = 2.5V |
| | | 51 @V _{GS} = 1.8V |

FEATURES

- Super high dense cell design for low R_{DS(ON)}.
- Rugged and reliable.
- SOT-23 package.
- Pb Free.



| ABSOLUTE MAXIMUM RATINGS (T _A = 25°C unless otherwise noted) | | | |
|---|-----------------------------------|------------|------|
| Parameter | Symbol | Limit | Unit |
| Drain-Source Voltage | V _{DS} | 20 | V |
| Gate-Source Voltage | V _{GS} | ±8 | V |
| Drain Current-Continuous @ T _c = 25°C | I _D | 3.77 | A |
| -Pulsed ^b | I _{DM} | 15 | A |
| Drain-Source Diode Forward Current ^a | I _S | 1.0 | A |
| Maximum Power Dissipation ^a | P _D | 1.25 | W |
| Operating Junction and Storage Temperature Range | T _J , T _{STG} | -55 to 150 | °C |
| THERMAL CHARACTERISTICS | | | |
| Thermal Resistance, Junction-to-Ambient ^a | R _{JA} | 100 | °C/W |

South Sea Semiconductor reserves the right to make changes to improve reliability or manufacturability without advance notice.

South Sea Semiconductor, September 2006 (Rev 2.0)



| Electrical Characteristics (T _A = 25°C unless otherwise noted) | | | | | | |
|---|---------------------|--|------|------------------|-------|------|
| Parameter | Symbol | Condition | Min | Typ ^c | Max | Unit |
| Drain-Source Breakdown Voltage | BV _{DSS} | V _{GS} =0V, I _D =250 μ A | 20 | | | V |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{DS} =16V, V _{GS} =0V | | | 1 | μ A |
| Gate-Body Leakage | I _{GSS} | V _{GS} = ± 8V, V _{DS} =0V | | | ± 100 | nA |
| Gate Threshold Voltage | V _{GS(th)} | V _{DS} =V _{GS} I _D =250 μ A | 0.45 | | 1.2 | V |
| Drain-Source On-State Resistance | R _{DS(ON)} | V _{GS} =4.5V, I _D =5.0A | | | 33 | m |
| | | V _{GS} =2.5V, I _D =4.5A | | | 40 | |
| | | V _{GS} =1.8V, I _D =4.0A | | | 51 | |
| On-State Drain Current | I _{D(ON)} | V _{DS} =10V, V _{GS} =4.5V | 15 | | | A |
| Forward Transconductance | g _{FS} | V _{DS} =15V, I _D =5A | | 40 | | S |
| Input Capacitance | C _{ISS} | V _{DS} =15V V _{GS} =0V f=1.0MHz | | 885 | | pF |
| Output Capacitance | C _{OSS} | | | 145 | | |
| Reverse Transfer Capacitance | C _{RSS} | | | 116 | | |
| Turn-On Delay Time | t _{D(ON)} | V _{DD} =10V, I _D =1A, V _{GS} =4.5V, R _{GEN} =6 Ω, R _L =10 Ω | | 16 | | ns |
| Rise Time | t _r | | | 38 | | |
| Turn-Off Delay Time | t _{D(OFF)} | | | 50.5 | | |
| Fall Time | t _f | | | 32 | | |
| Total Gate Charge | Q _g | V _{DS} =10V, I _D =5A, V _{GS} =4.5V | | 11 | | nC |
| Gate-Source Charge | Q _{gs} | | | 1.4 | | |
| Gate-Drain Charge | Q _{gd} | | | 2.2 | | |
| Diode Forward Voltage | V _{SD} | V _{GS} =0V, I _D =1A | | 0.8 | 1.2 | V |

Notes :

- a. Surface Mounted on FR4 Board, t ≤ 10 sec.
- b. Pulse Test : Pulse Width ≤ 300 μ s, Duty Cycle ≤ 2%.
- c. Guaranteed by design, not subject to production testing.

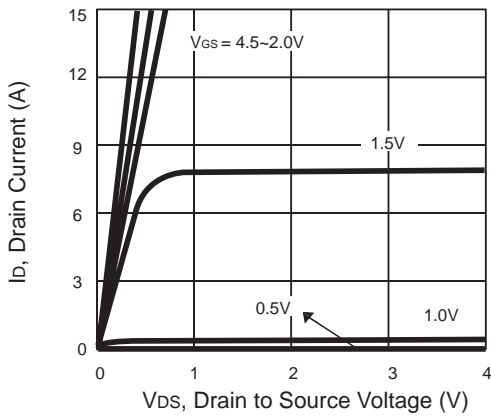


Figure 1. Output Characteristics

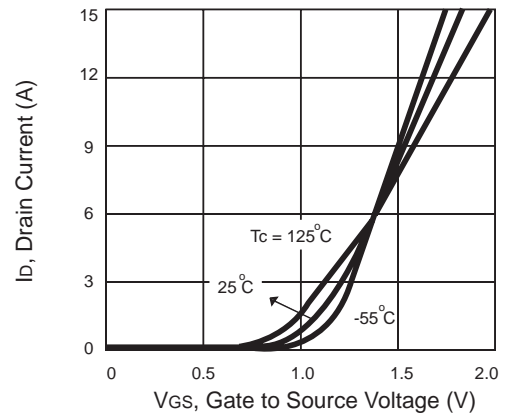


Figure 2. Transfer Characteristics

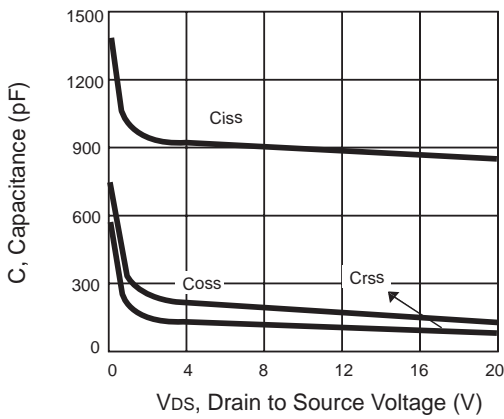


Figure 3. Capacitance

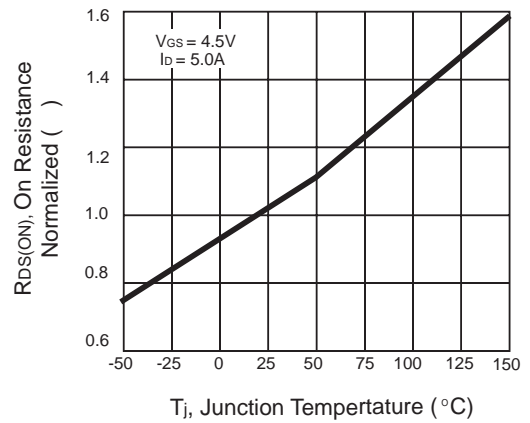


Figure 4. On Resistance Variation with Junction Temperature

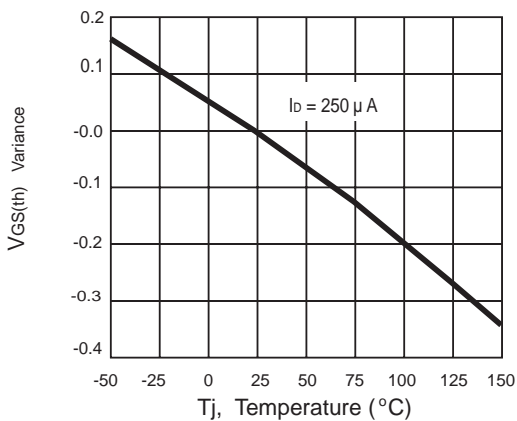


Figure 5. Threshold Voltage

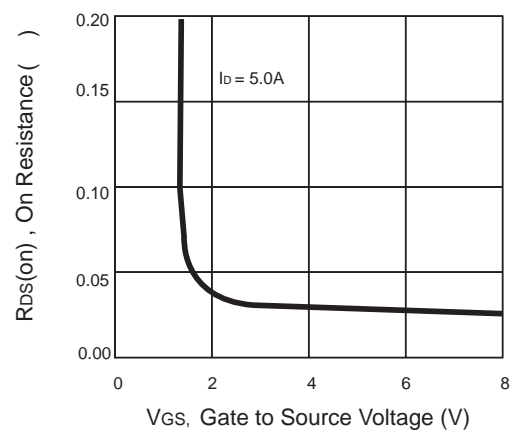


Figure 6. On Resistance Variation with Gate to Source Voltage

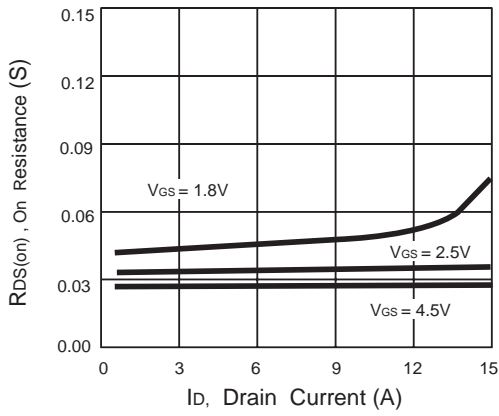


Figure 7. On Resistance Variation with Drain Current

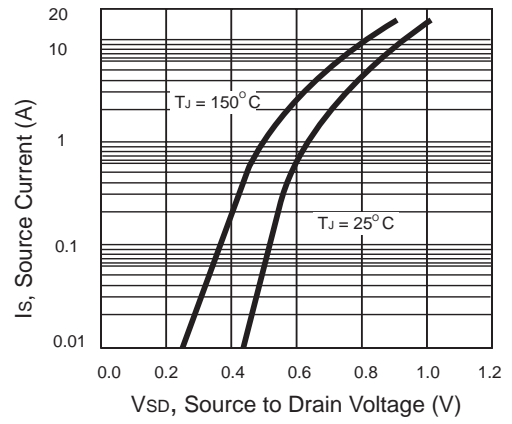


Figure 8. Source Drain Diode Forward Voltage

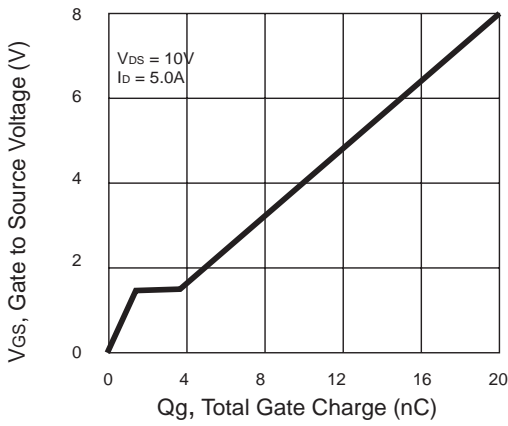


Figure 9. Gate Charge

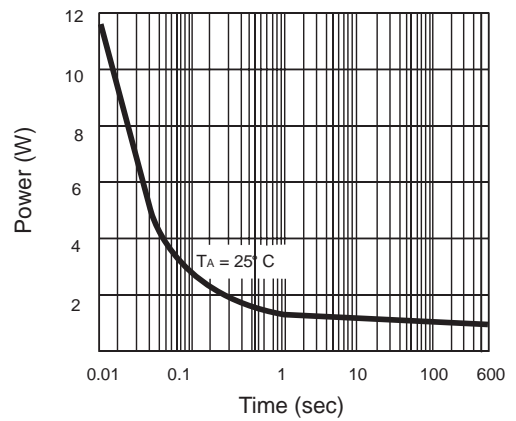


Figure 10. Single Pulse Power

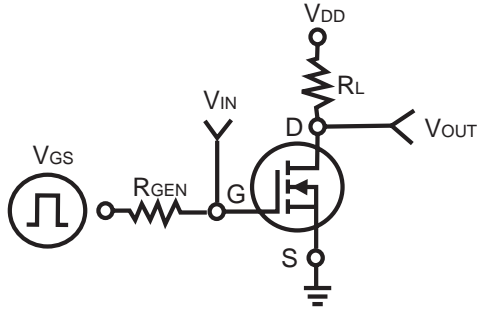


Figure 11. Switching Test Circuit

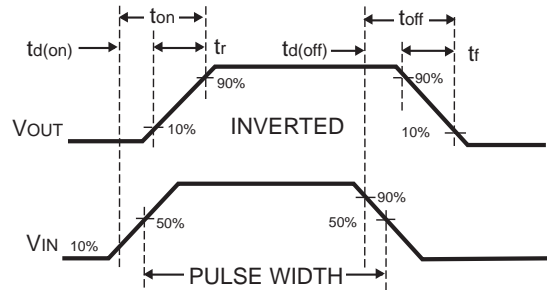


Figure 12. Switching Waveforms

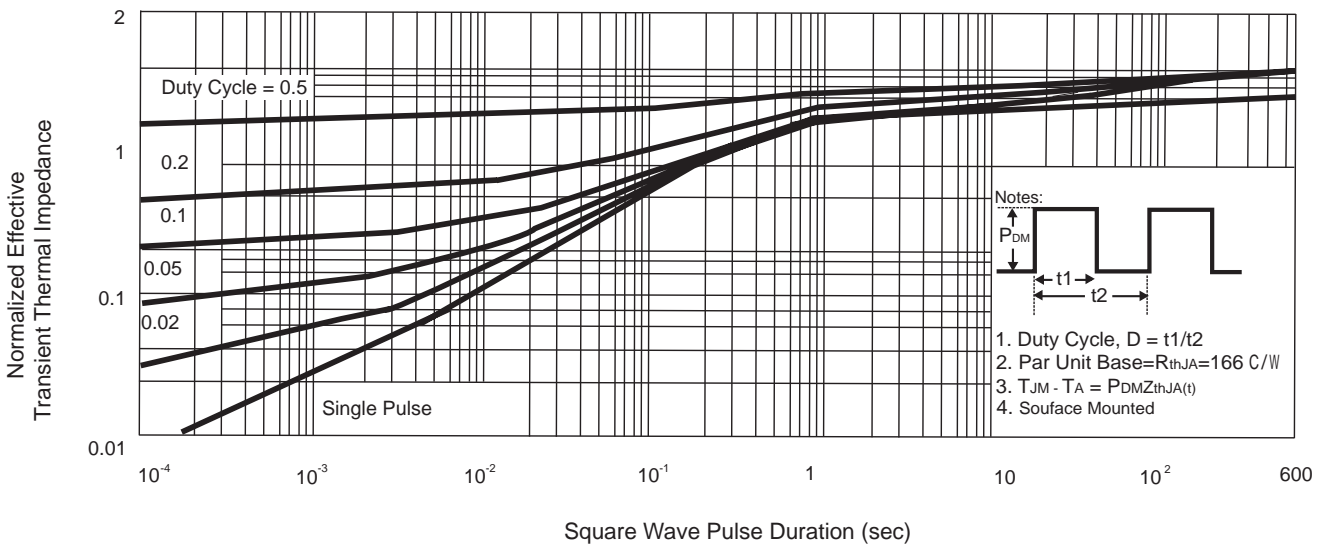


Figure 13. Normalized Thermal Transient Impedance, Junction to Ambient