



South Sea Semiconductor

# SSN2N7002A

## N-Channel Enhancement Mode MOSFET

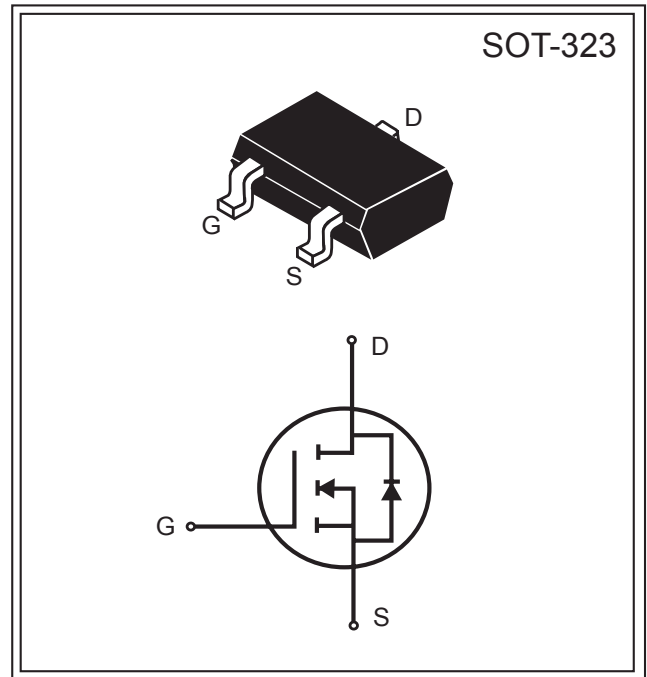
### Product Summary

$V_{DS}$ (V)	$I_D$ (A)	$R_{DS(ON)}$ ( $\Omega$ ) Max
60V	0.25A	3 @ $V_{GS} = 10V$
		4 @ $V_{GS} = 5V$

### FEATURES

- ◆ Super high dense cell design for low  $R_{DS(ON)}$ .
- ◆ Rugged and reliable.
- ◆ SOT-323 package.

Marking Code : 2A



### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous @ $T_J = 125^\circ C$	$I_D$	250	mA
-Pulsed <sup>b</sup>	$I_{DM}$	1	A
Drain-Source Diode Forward Current <sup>a</sup>	$I_S$	250	mA
Maximum Power Dissipation <sup>a</sup>	$P_D$	200	mW
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^\circ C$

### THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient <sup>a</sup>	$R_{\theta JA}$	625	$^\circ C/W$
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South Sea Semiconductor reserves the right to make changes to improve reliability or manufacturability without advance notice.

South Sea Semiconductor, December 2007 (Rev 3.0)



N-Channel Electrical Characteristics (T <sub>A</sub> = 25°C unless otherwise noted)						
Parameter	Symbol	Condition	Min	Typ <sup>c</sup>	Max	Unit
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =10 μA	60			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V			1	μA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> I <sub>D</sub> =250 μA	1	2	2.5	V
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =250mA		2.0	3.0	Ω
		V <sub>GS</sub> = 5V, I <sub>D</sub> =50mA		3.0	4.0	
On-State Drain Current	I <sub>D(on)</sub>	V <sub>DS</sub> =7V, V <sub>GS</sub> =10V	495			mA
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =7V, I <sub>D</sub> =200mA	78			mS
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =25V		20	50	pF
Output Capacitance	C <sub>OSS</sub>	V <sub>GS</sub> =0V		11	25	
Reverse Transfer Capacitance	C <sub>RSS</sub>	f=1.0MHz		2.5	5	
Turn-On Delay Time	t <sub>D(on)</sub>	V <sub>DD</sub> =30V, I <sub>D</sub> =100mA, V <sub>GS</sub> =10V, R <sub>GEN</sub> =10Ω		7.8	20	ns
Rise Time	t <sub>r</sub>			5.5		
Turn-Off Delay Time	t <sub>D(off)</sub>			7.8	20	
Fall Time	t <sub>f</sub>			2.8		
Diode-Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250mA		0.75	1.5	V

## Notes :

- Surface Mounted on FR4 Board, t ≤ 10 sec.
- Pulse Test : Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
- Guaranteed by design, not subject to production testing.

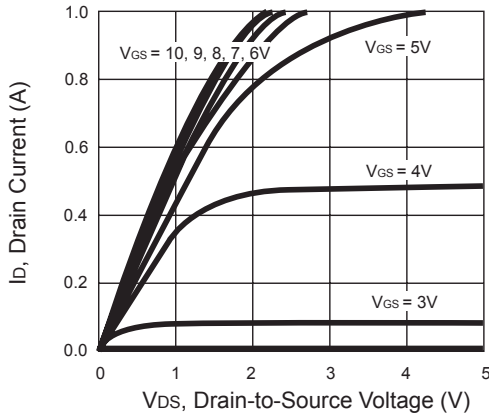


Figure 1. Output Characteristics

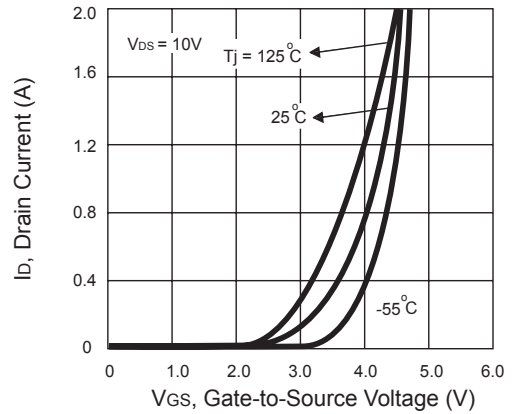


Figure 2. Transfer Characteristics

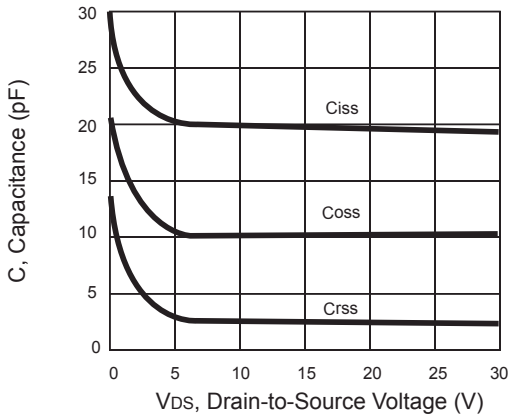


Figure 3. Capacitance

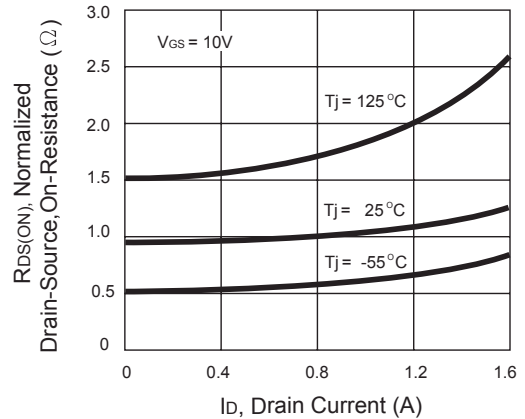


Figure 4. On-Resistance Variation with Temperature

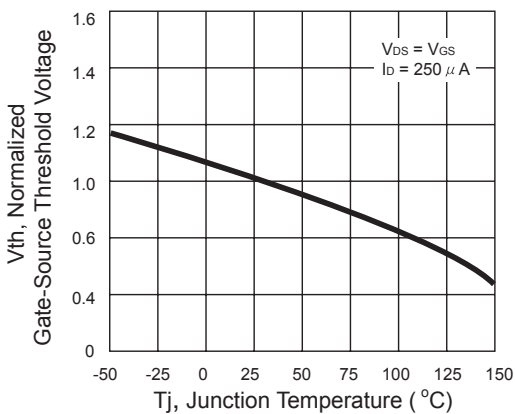


Figure 5. Gate Threshold Variation with Temperature

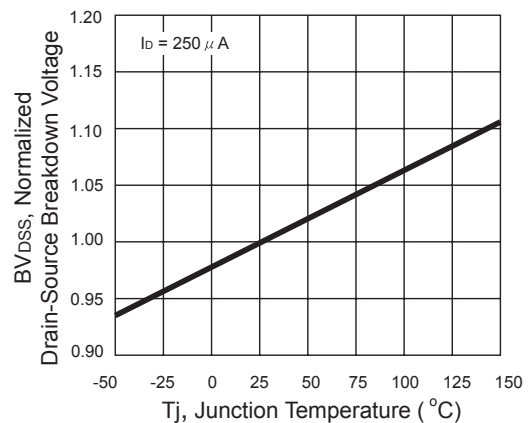
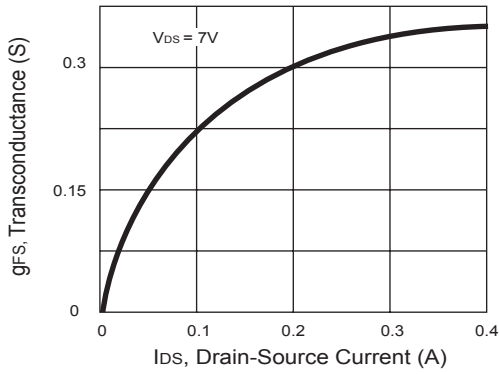
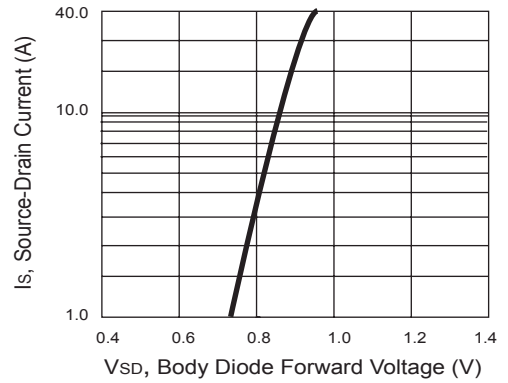


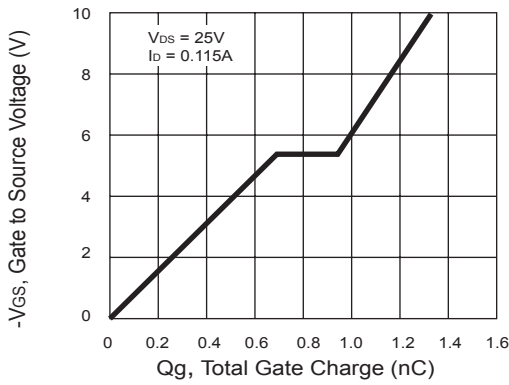
Figure 6. Breakdown Voltage Variation with Temperature



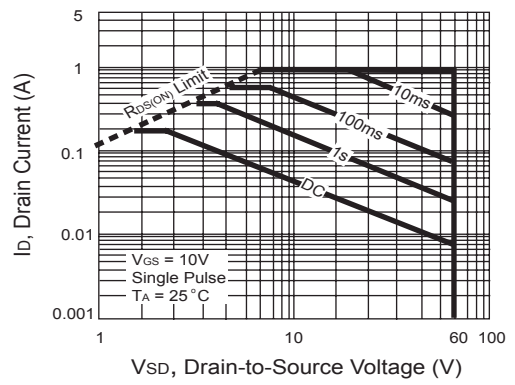
**Figure 7. Transconductance Variation with Drain Current**



**Figure 8. Body Diode Forward Voltage Variation with Source Current**



**Figure 9. Gate Charge**



**Figure 10. Maximum Safe Operating Area**

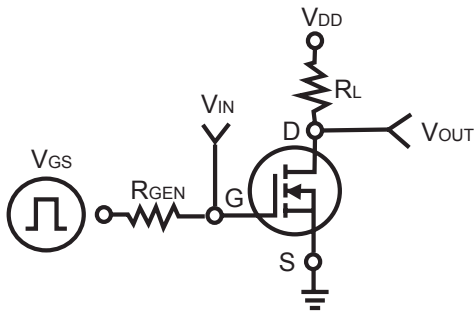


Figure 11. Switching Test Circuit

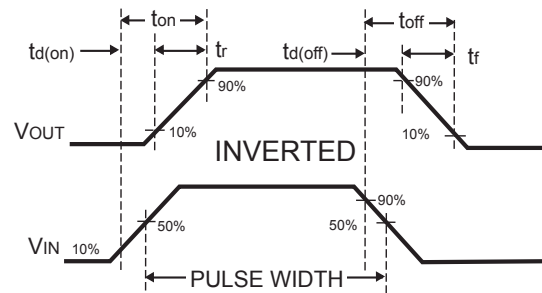


Figure 12. Switching Waveforms

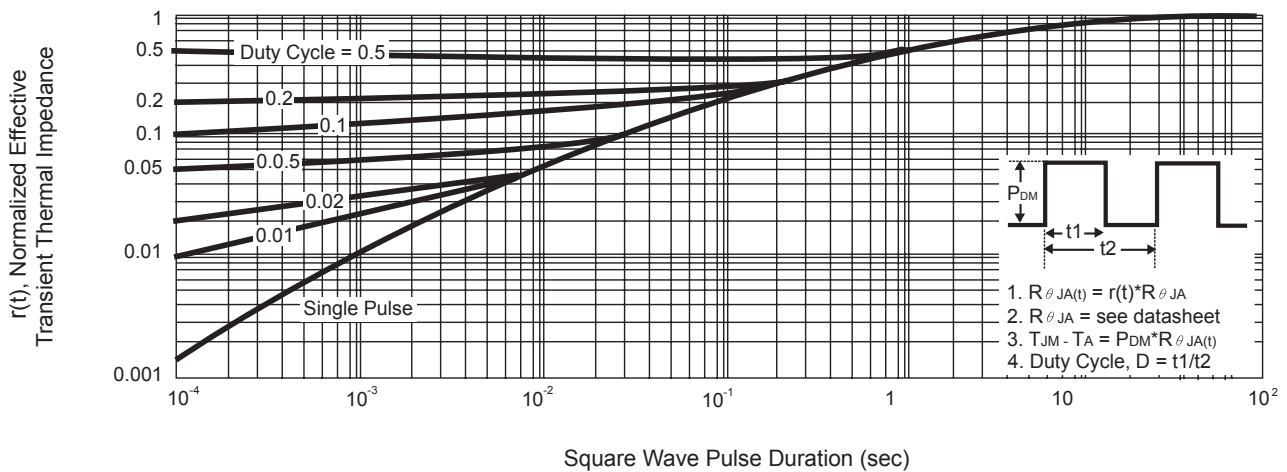
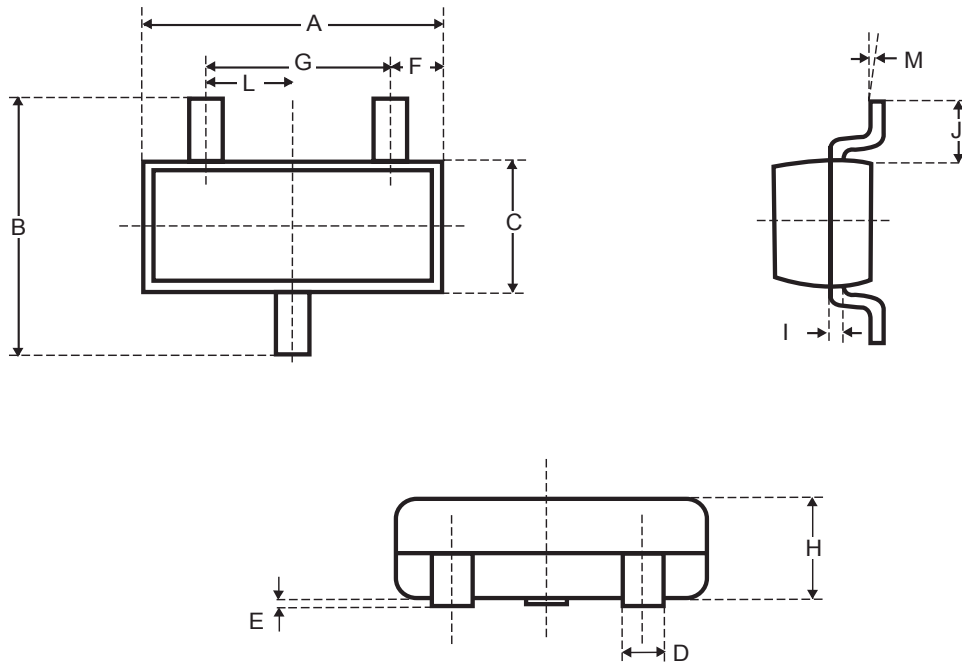


Figure 13. Normalized Thermal Transient Impedance Curve



# Package Outline Dimensions

SOT-323



SYMBOLS	MILLIMETERS		INCHES	
	Min.	Max.	Min.	Max.
A	1.80	2.20	0.070	0.087
B	2.00	2.20	0.094	0.110
C	1.15	1.35	0.045	0.054
D	0.20	0.40	0.016	0.0078
E	0	0.10	0	0.004
F	0.30	0.40	0.0115	0.0155
G	1.20	1.40	0.047	0.056
H	0.90	1.10	0.035	0.044
I	0.05	0.15	0.002	0.006
J	0.40	0.425	0.016	0.167
L	0.60	0.70	0.0235	0.028
M	0°	10°	0°	10°