



South Sea Semiconductor

SSN2N7002C

Dual Enhancement Mode MOSFET

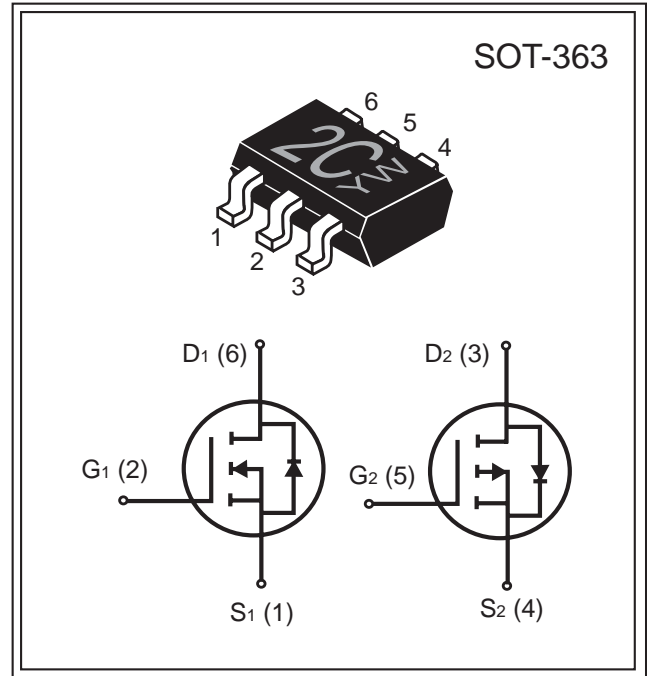
Product Summary (N-Channel)		
V _{DS} (V)	I _D (A)	R _{DS(ON)} () Max
60V	0.120A	3.0 @V _{GS} = 10V
		4.0 @V _{GS} = 4.5V

Product Summary (P-Channel)		
V _{DS} (V)	I _D (A)	R _{DS(ON)} () Max
-60V	-0.130A	7.5 @V _{GS} = 10V
		10.0 @V _{GS} = 4.5V

FEATURES

- Super high dense cell design for low R_{DS(ON)}.
- Rugged and reliable.
- SOT-363 package.
- Pb Free.

Marking Code : 2C



ABSOLUTE MAXIMUM RATINGS (T_A = 25 C unless otherwise noted)

Parameter	Symbol	N-Channel Limited	P-Channel Limited	Unit
Drain-Source Voltage	V _{DS}	60	-60	V
Gate-Source Voltage	V _{GS}	± 20	± 20	V
Drain Current-Continuous @ T _J = 125 °C	I _D	120	-130	mA
-Pulsed ^b	I _{DM}	1	-1	A
Drain-Source Diode Forward Current ^a	I _S	130	-130	mA
Maximum Power Dissipation ^a	P _D	200		mW
Operating Junction and Storage Temperature Range	T _J , T _{STG}	-55 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient ^a	R _{JA}	625	°C/W
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South Sea Semiconductor reserves the right to make changes to improve reliability or manufacturability without advance notice.

South Sea Semiconductor, October 2006 (Rev 2.0)



N-Channel Electrical Characteristics (TA = 25°C unless otherwise noted)						
Parameter	Symbol	Condition	Min	Typ ^c	Max	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =10 μ A	60			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V			1	μ A
Gate-Body Leakage	I _{GSS}	V _{GS} = ± 20V, V _{DS} =0V			± 10	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} I _D =250 μ A	1	1.6	2.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =500mA			3	
		V _{GS} = 5V, I _D =50mA			4	
On-State Drain Current	I _{D(ON)}	V _{DS} =7.5V, V _{GS} =10V	495	1650		mA
Forward Transconductance	g _{FS}	V _{DS} =10V, I _D =200mA	78			mS
Input Capacitance	C _{ISS}	V _{DS} =25V			50	pF
Output Capacitance	C _{OSS}	V _{GS} =0V			25	
Reverse Transfer Capacitance	C _{RSS}	f=1.0MHz			5	
Turn-On Delay Time	t _{D(ON)}	V _{DD} =30V,		7.8	20	ns
Rise Time	t _r	I _D =200mA,		5.5		
Turn-Off Delay Time	t _{D(OFF)}	V _{GS} =10V,		7.8	20	
Fall Time	t _f	R _{GEN} =25		2.8		
Diode-Forward Voltage	V _{SD}	V _{GS} =0V, I _D =250mA		0.75	1.5	V

Notes :

- a. Surface Mounted on FR4 Board, t ≤ 10 sec.
- b. Pulse Test : Pulse Width ≤ 300 μ s, Duty Cycle ≤ 2%.
- c. Guaranteed by design, not subject to production testing.



P-Channel Electrical Characteristics (T _A = 25°C unless otherwise noted)						
Parameter	Symbol	Condition	Min	Typ ^c	Max	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-10 μA	-60			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-60V, V _{GS} =0V			-1	μA
Gate-Body Leakage	I _{GSS}	V _{GS} = ± 20V, V _{DS} =0V			± 10	μA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} I _D =-250 μA	-1		-3	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =-10V, I _D =-0.5A			7.5	
		V _{GS} = -4.5V, I _D =-0.025A			10	
On-State Drain Current	I _{D(ON)}	V _{DS} =-10V, V _{GS} =-10V	600			mA
Forward Transconductance	g _{FS}	V _{DS} =-10V, I _D =-0.1A		430		mS
Input Capacitance	C _{ISS}	V _{DS} =-25V V _{GS} =0V f=1.0MHz		80		pF
Output Capacitance	C _{OSS}			11		
Reverse Transfer Capacitance	C _{RSS}			4		
Turn-On Delay Time	t _{D(ON)}	V _{DD} =-25V, I _D =-120mA, V _{GS} =-10V, R _{GEN} =6		2.8		ns
Rise Time	t _r			6.5		
Turn-Off Delay Time	t _{D(OFF)}			10		
Fall Time	t _f			7.2		
Diode-Forward Voltage	V _{SD}	V _{GS} =0V, I _D =-200mA		-0.75	-1.4	V

Notes :

- a. Surface Mounted on FR4 Board, t ≤ 10 sec.
- b. Pulse Test : Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
- c. Guaranteed by design, not subject to production testing.



N-Channel

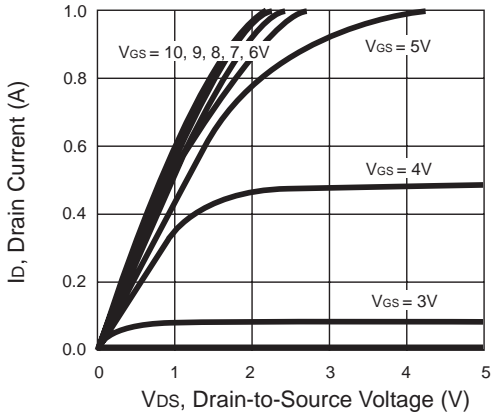


Figure 1. Output Characteristics

P-Channel

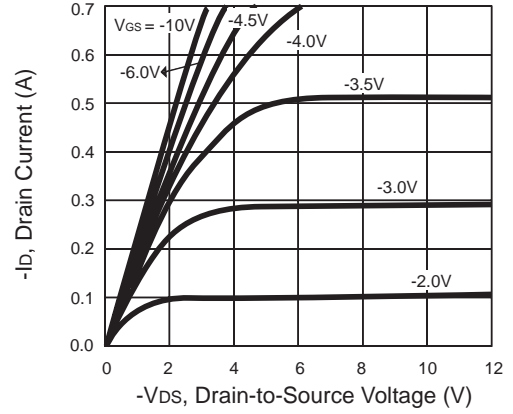


Figure 1. Output Characteristics

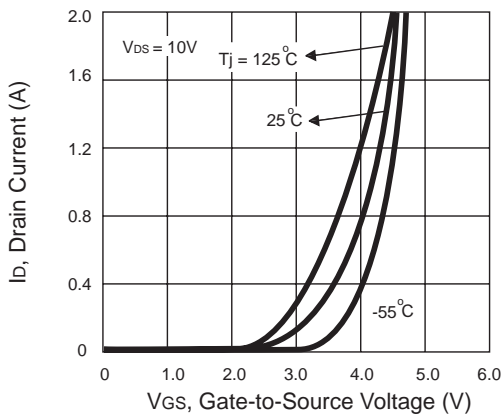


Figure 2. Transfer Characteristics

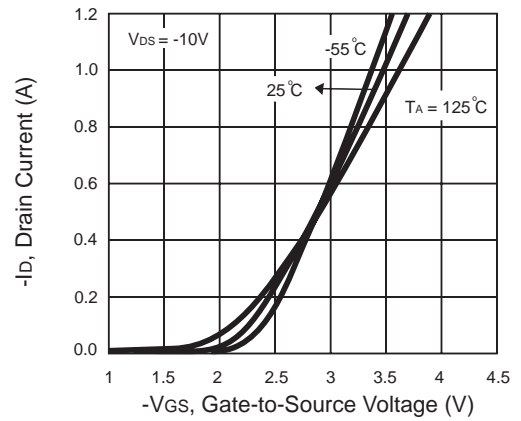


Figure 2. Transfer Characteristics

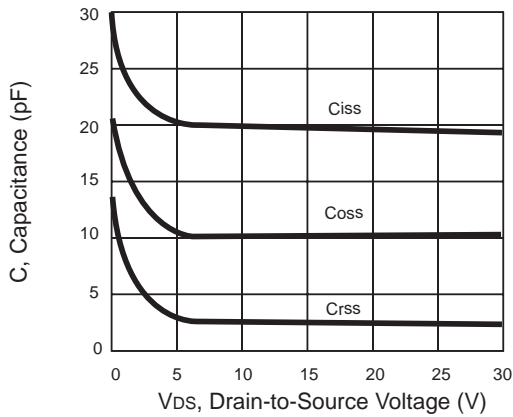


Figure 3. Capacitance

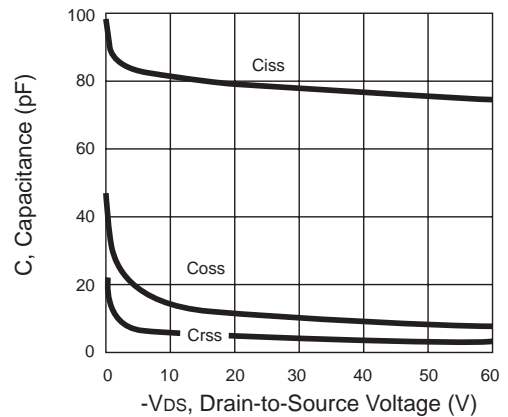


Figure 3. Capacitance



N-Channel

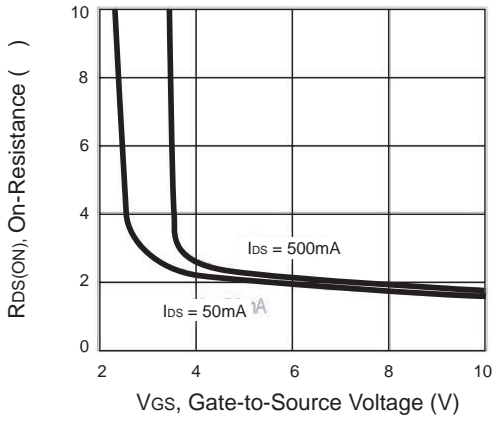


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

P-Channel

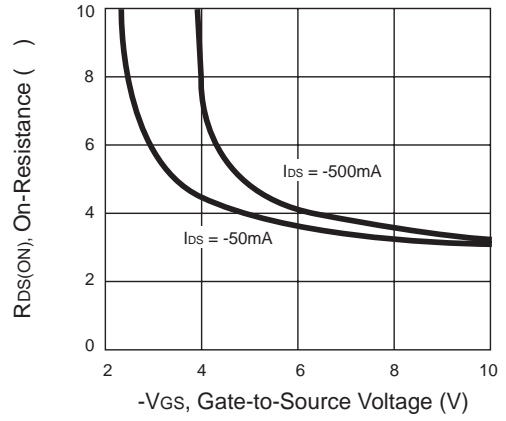


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

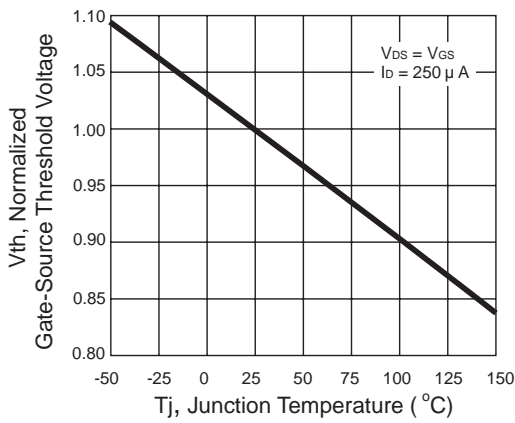


Figure 5. Gate Threshold Variation with Temperature

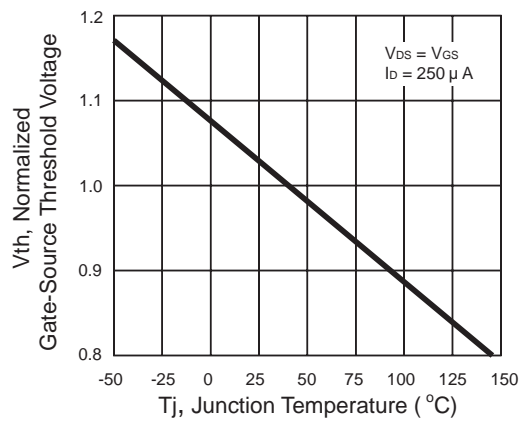


Figure 5. Gate Threshold Variation with Temperature

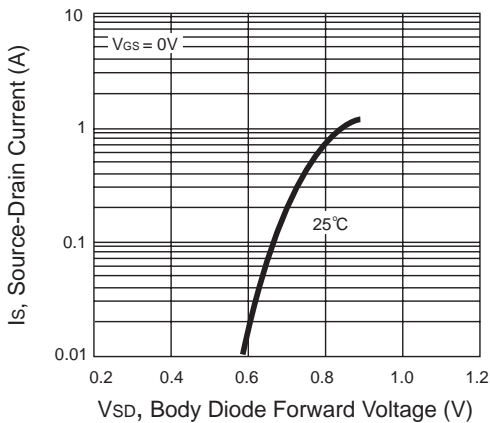


Figure 6. Body Diode Forward Voltage Variation with Source Current

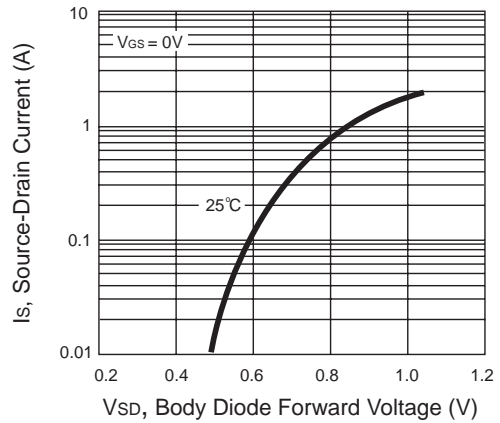


Figure 6. Body Diode Forward Voltage Variation with Source Current