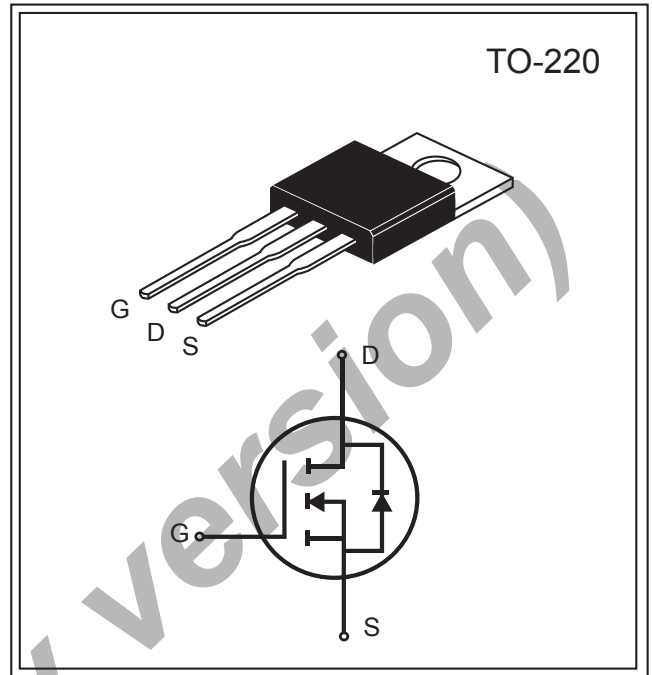




# SSP4070NL

## N-Channel Enhancement Mode MOSFET

Product Summary		
$V_{DS}$ (V)	$I_D$ (A)	$R_{DS(ON)}$ (m $\Omega$ ) Max
70V	40A	50 @ $V_{GS} = 10V$
		80 @ $V_{GS} = 5V$



### FEATURES

- ◆ Super high density cell design for low  $R_{DS(ON)}$ .
- ◆ Rugged and reliable.
- ◆ TO-220 package.
- ◆ Pb free.

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	70	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous @ $T_C = 25^\circ\text{C}$	$I_D$	40	A
-Pulsed <sup>b</sup>	$I_{DM}$	100	A
Drain-Source Diode Forward Current <sup>a</sup>	$I_S$	20	A
Maximum Power Dissipation <sup>a</sup> @ $T_C = 25^\circ\text{C}$	$P_D$	75	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.0	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient <sup>a</sup>	$R_{\theta JA}$	62	

South Sea Semiconductor reserves the right to make changes to improve reliability or manufacturability without advance notice.

South Sea Semiconductor, April 2008 (Rev 1.0)



Electrical Characteristics (TA = 25°C unless otherwise noted)						
Parameter	Symbol	Condition	Min	Typ <sup>c</sup>	Max	Unit
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250 μA	70			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V			1	μA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250 μA	1	1.8	3	V
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =25A		42	50	mΩ
		V <sub>GS</sub> =5V, I <sub>D</sub> =15A		72	80	
On-State Drain Current	I <sub>D(on)</sub>	V <sub>DS</sub> =10V, V <sub>GS</sub> =10V	40			A
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =15A		9		S
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =25V		1100		pF
Output Capacitance	C <sub>OSS</sub>	V <sub>GS</sub> =0V		160		
Reverse Transfer Capacitance	C <sub>RSS</sub>	f=1.0MHz		60		
Turn-On Delay Time	t <sub>D(on)</sub>	V <sub>DD</sub> =30V,		30		ns
Rise Time	t <sub>r</sub>	I <sub>D</sub> =20A,		80		
Turn-Off Delay Time	t <sub>D(off)</sub>	V <sub>GS</sub> =10V,		27		
Fall Time	t <sub>f</sub>	R <sub>GEN</sub> =6Ω		40		
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =30V, I <sub>D</sub> =20A, V <sub>GS</sub> =5V		8		nC
Gate-Source Charge	Q <sub>gs</sub>			2		
Gate-Drain Charge	Q <sub>gd</sub>			2.5		
Diode Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =20A			1.4	V

## Notes :

- Surface Mounted on FR4 Board, t ≤ 10 sec.
- Pulse Test : Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
- Guaranteed by design, not subject to production testing.

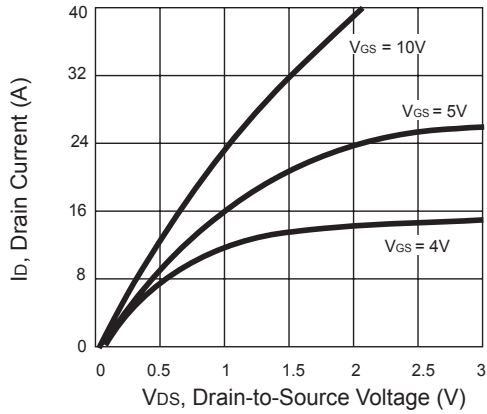


Figure 1. Output Characteristics

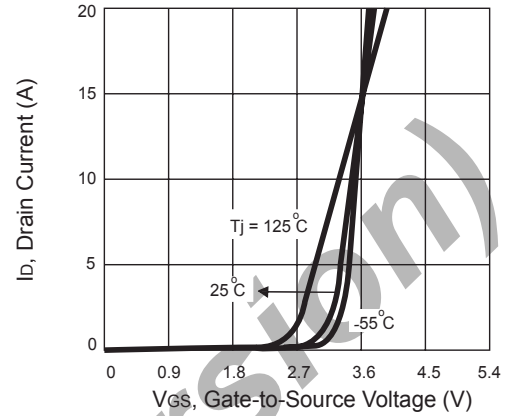


Figure 2. Transfer Characteristics

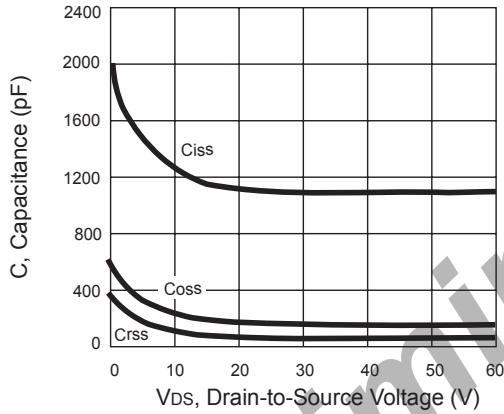


Figure 3. Capacitance

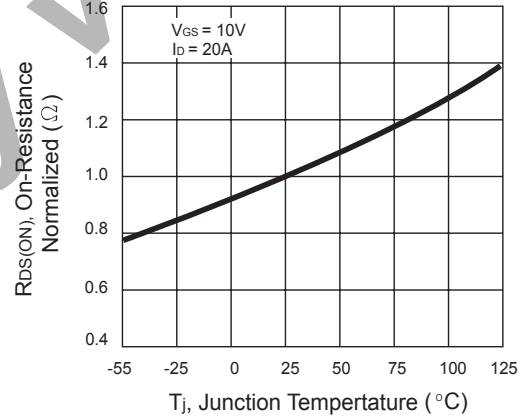


Figure 4. On-Resistance Variation with Temperature

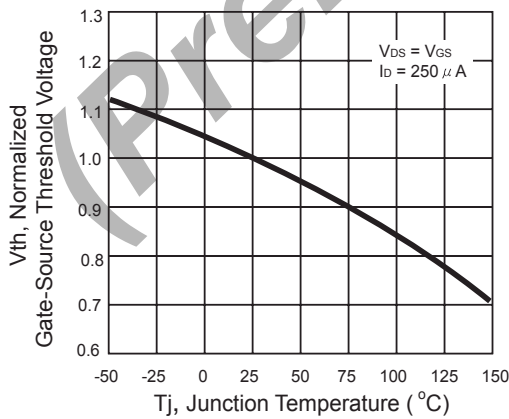


Figure 5. Gate Threshold Variation with Temperature

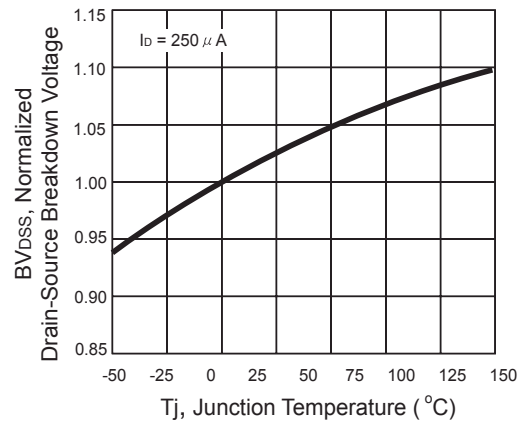


Figure 6. Breakdown Voltage Variation with Temperature

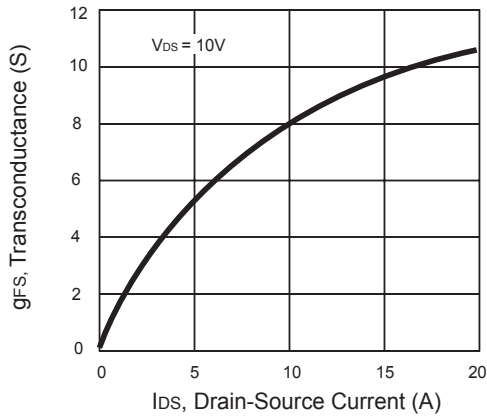


Figure 7. Transconductance Variation with Drain Current

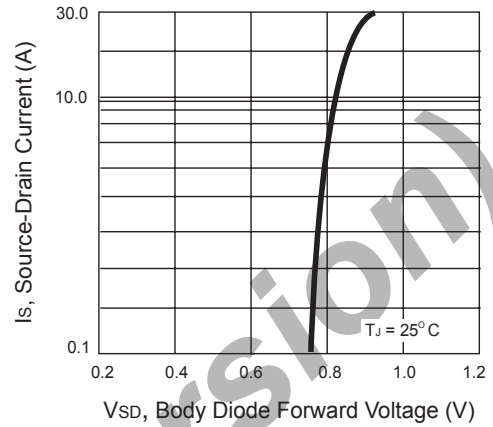


Figure 8. Body Diode Forward Voltage Variation with Source Current

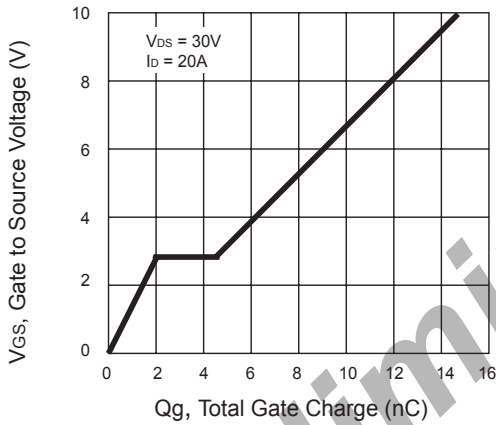


Figure 9. Gate Charge

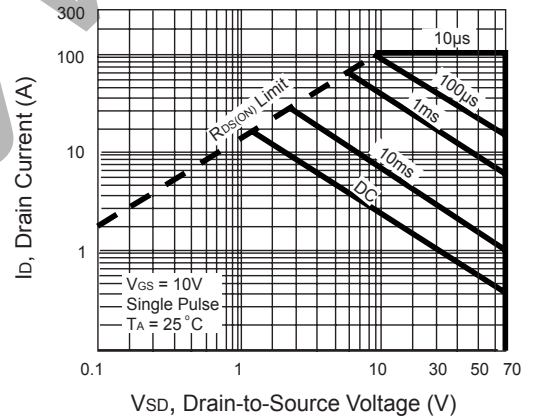


Figure 10. Maximum Safe Operating Area

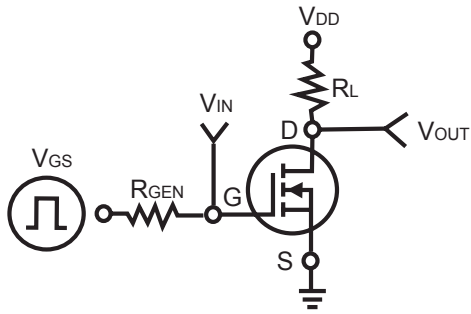


Figure 11. Switching Test Circuit

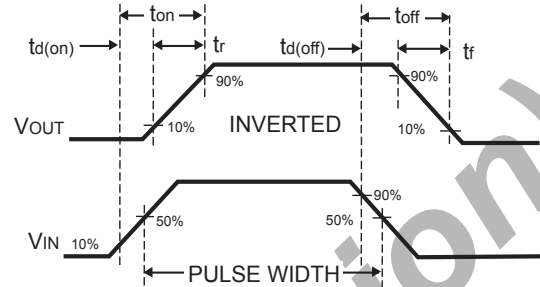


Figure 12. Switching Waveforms

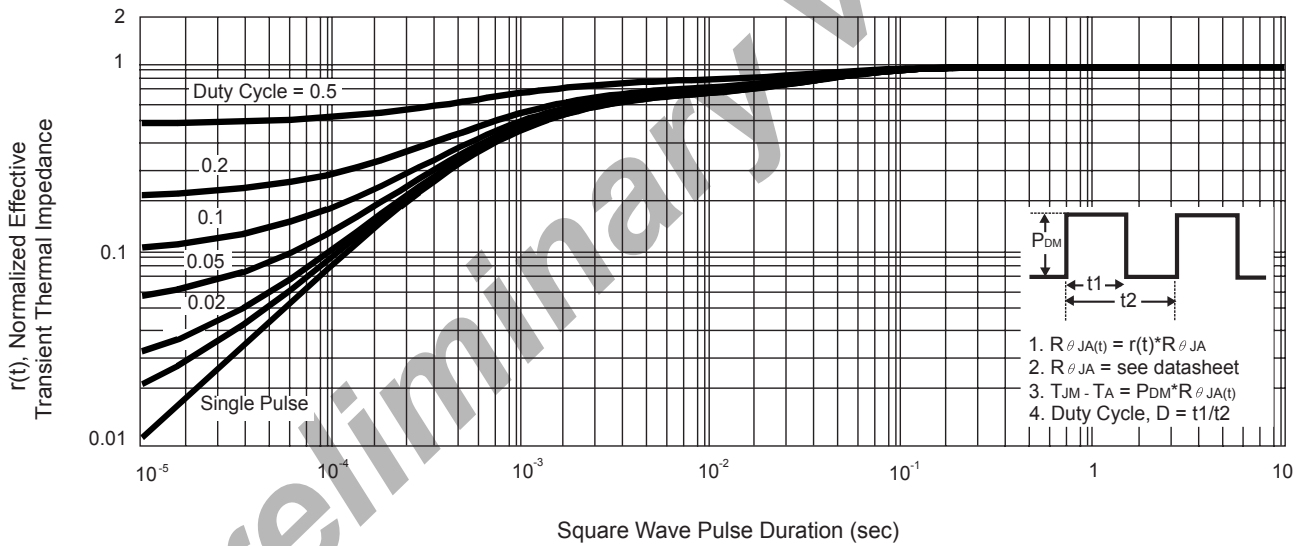


Figure 13. Normalized Thermal Transient Impedance Curve